A High Power Density Power Factor Correction Converter With a Multilevel Boost Front-End and a Series-Stacked Energy Decoupling Buffer

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***Abstract*—High efficiency and high power density Power Factor Correction (PFC) converters are desirable in many ac-dc applications such as data center power delivery and electric vehicle on-board chargers. In conventional boost converter based PFC designs, two of the major limitations to achieve high power density are the size of the input filter inductor of the boost converter and the twice-line frequency energy buffering capacitor bank. In this work, a 1.5 kW universal ac (95 to 265 Vac) input, 400 V dc output PFC converter with a flying capacitor multilevel (FCML) boost front-end and a series-stacked buffer (SSB) is implemented to improve the overall system power density and efficiency. The unique challenges in both hardware and digital controller designs to achieve the co-operation of PFC, FCML and SSB are addressed, and corresponding solutions are presented in detail.**

I. Introduction

Power factor correction (PFC) converters are widely used in grid-connected ac-dc conversion applications to improve the power quality and efficiency. A conventional design usually features a boost converter to rectify and control the power factor of the input ac voltage and current, and a large electrolytic capacitor bank on the dc output side to process the twice-line frequency pulsating power and maintain a small voltage ripple on the dc-bus. In such design, the size of the input inductor of the boost converter suffers from large voltage stress and low switching frequency [1]. Alternative two-level front-end topologies such as totem-pole PFC [2] provides some benefits over conventional boost topology, such as lower conduction loss, lower switching loss (if soft switching and GaN switches are implemented [2]), and fewer device count, among others. However, they do not reduce the required inductor size, and have limited frequency of operation for reasonable loss. On the dc output side, due to the small voltage ripple requirements on the dc-bus voltage, the twice-line frequency energy buffering electrolytic capacitor bank often results in large physical volume. The boost inductors and twice-line frequency buffering capacitors thus are the two major barriers to improve the power density of boost converter based PFC converters. In this work, a 1.5 kW universal ac input, 400 V dc output PFC converter with the architecture shown in Fig. 1 is proposed and built to overcome these two barriers to improve the system power density, while simutaneously enabling ultra high efficiency.

To reduced the input inductor size, the PFC front-end in this work is designed with flying capacitor multilevel (FCML) boost topology. FCML converters utilize high energy density capacitors to facilitate the energy transfer during the conversion process, thus the total passive component volume in the converter is significantly reduced [3]. The Series-Stacked Buffer (SSB) is a type of active energy decoupling device in single-phase converters, which has demonstrated high power density and high efficiency in the inverter system in [4], [5]. As shown in Fig. 1, in this architecture, a buffer converter is connected in series with the main energy buffering capacitor C_1, which stores and releases energy with a large voltage ripple, allowing a high energy utilization ratio to reduce the required capacitance, compared to the passive capacitor bank solution. The buffer converter in series is controlled to generate a voltage that cancels the ripple on C_1 such that the dc-bus voltage has no twice-line frequency ripple content.

The first high power density, high efficiency single-phase inverter system with FCML inverter stage and SSB buffer has been demonstrated in [5]. As this architecture showed great promises to improve the performance of single-phase converters, research efforts have been made to further improve the performance, solve fundamental issues, and optimize the component sizing of both the FCML and SSB. This work, first of all, is the first demonstration of this architecture used in a single-phase PFC system. As such, unique challenges in system control for this architecture in PFC applications will be addressed. Furthermore, it is also a test platform to integrate some of the recently proposed hardware design and digital control techniques to improve both FCML and SSB that have not been implemented simultaneously in a complete ac-dc PFC system.

Specifically, for the FCML stage:

1) The cascaded bootstrap method is used to provide floating gate driving power [6], which is more efficient and smaller than the isolated dc-dc solution in [5].
2) 6-level, instead of 7-level FCML is designed. This is based on the fundamental analysis in [7] that even-level FCMLs have better flying capacitor voltage balancing characteristics than odd-level FCMLs.
3) The small inductor in the FCML boost causes the input

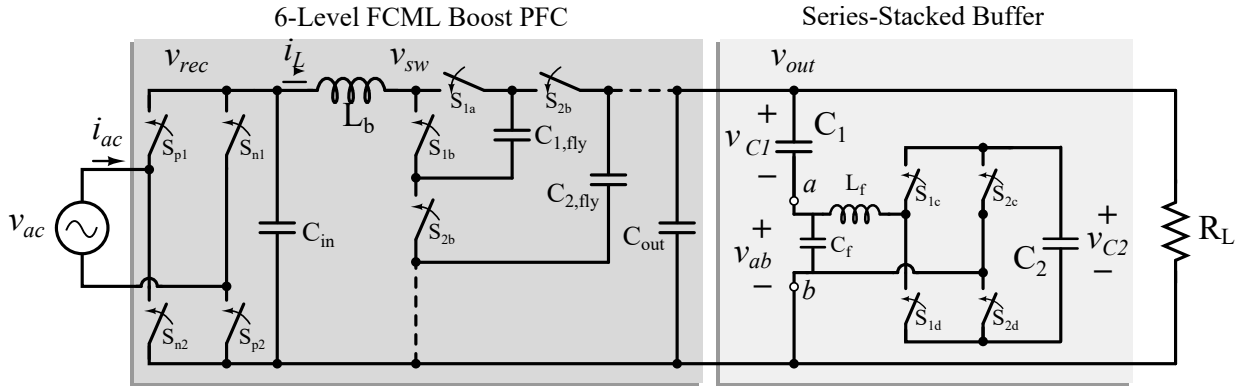

Fig. 1: System architecture of the proposed PFC converter.

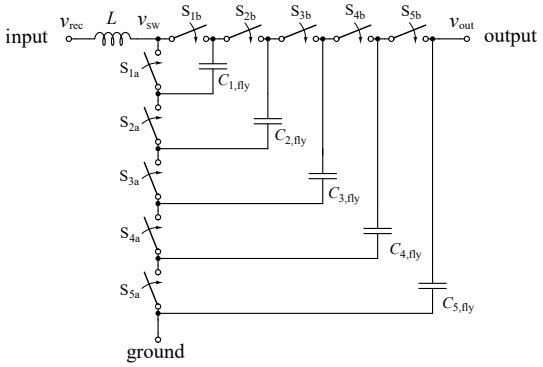

Fig. 2: Schematic drawing of a 6-level FCML boost converter.

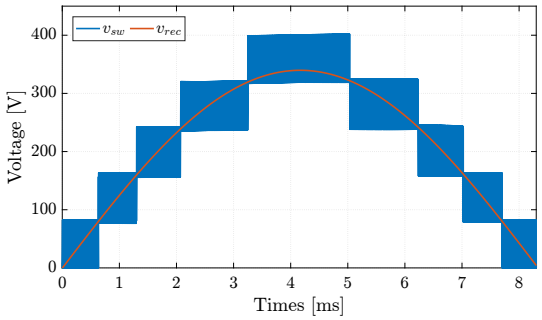

Fig. 3: Exemplar 6-level FCML switching node waveform with 240 V_{rms} rectified sine input and 400 V output.

current to be more sensitive to input voltage disturbance in PFC applications. To solve this issue, the partial feedforward control is used to improve the input power factor [8].

For the SSB:

1) The updated design constraints [9] and multi-objective optimization analysis [10] allow much more optimized passive component sizing compared to the conservative design in [4], [5], resulting in more than 15% increase in power density.
2) Compared to the current controlled method in [4], [5], a simpler voltage controlled scheme is developed based on the impedance modeling for SSB [11]. Improving upon the voltage controlled scheme, the proposed PLL-based control technique for SSB in this work further simplifies the digital controller and ensures system stability in PFC operation.

This paper first introduces FCML and SSB in general, and how the aforementioned techniques are applied to the design. Then the particular control scheme of the PFC system is addressed. Lastly, the experiment results of 240 Vac and 120 Vac input to 400 Vdc conversions are provided and analyzed.

II. System Architecture

A. FCML Boost PFC Front-End

As shown in Fig. 3, the line voltage input v_{ac} is processed by an active full bridge rectifier commuting at line frequency to generate a rectified sine wave v_{rec}, which is then boosted by the 6-level FCML converter to a constant output voltage v_{out}. The FCML boost converter shown in Fig. 2 can greatly alleviate the problems of the conventional boost converter such as the large volume of the magnetic components, high voltage stress on the transistors and EMI challenges. An in-depth comparison between these two topologies can be found in [3].

Each switch in the FCML is controlled by a pulse width modulation (PWM) signal with a duty ratio of D, and is phase-shifted by $\frac{360^\circ}{N-1}$ from the adjacent PWM signals, i.e., D for all low side transistors S_{1a} to $S_{(N-1)a}$ and $1-D$ for all high side transistors S_{1b} to $S_{(N-1)b}$), and is phase-shifted by $\frac{360^\circ}{N-1}$ from the adjacent PWM signals. In the steady state, the N-level FCML boost converter naturally balances the voltages across $(N-2)$ flying capacitors, each of which holds voltage of $\frac{V_{out}}{N-1}$, $\frac{2V_{out}}{N-1}$, ..., $\frac{(N-2)V_{out}}{N-1}$ [12]. For example, in the 6-level FCML converter shown in Fig. 2, $C_{fly,\,1}$ has a voltage of $\frac{V_{out}}{5}$, $C_{fly,\,2}$ has a voltage of $\frac{2V_{out}}{5}$, etc. Moreover, compared to the 7-level FCML inverter in [5], the 6-level FCML converter is more immune to disturbances on the flying capacitor voltages, thanks to the mutual balancing mechanism in even-level FCML converters

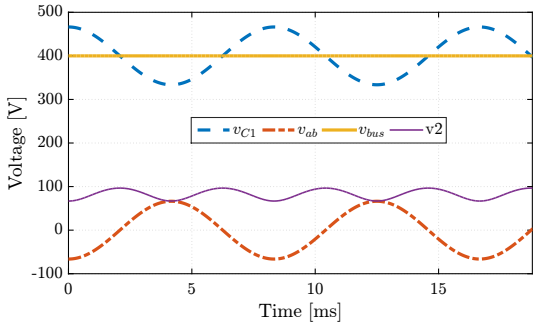

Fig. 4: Exemplar voltage waveform of SSB in normal operation for 1.5 kW load and 400 V dc-bus.

[7]. An exemplar 6-level FCML switching node voltage v_{sw} resulted from a rectified sine input voltage in PFC application is presented in Fig. 3.

Compared to a conventional boost converter with the same inductor current ripple, since the voltage ripple seen by the inductor is reduced by a factor of five while the frequency seen by the inductor is increased by a factor of five, the filter inductor of the 6-level converter can be reduced by a factor of 25 as a first order estimation.

B. Series-Stacked Buffer

If the input ac voltage $v_{ac} = V_{ac} sin(\omega t)$ and input current $i_{ac} = I_{ac} sin(\omega t)$ (ω = 2$\pi\times$ 60 rad/s) are controlled to be in phase by the PFC controller, the instantaneous input ac power is expressed as

$$p_{in} = v_{ac} i_{ac} = \frac{V_{ac} I_{ac}}{2}(1 - cos(2\omega t)) = P_0(1 - cos(2\omega t)). \quad (1)$$

The instantaneous power processed by the SSB is purely reactive, i.e., $p_{buf} = -P_0 cos(2\omega t)$, where P_0 is the rated output power. Assuming negligible ripple on V_{out}, the current flowing into the SSB can be derived as

$$i_{buf} = \frac{p_{buf}}{V_{out}} = \frac{-P_0}{V_{out}} cos(2\omega t). \quad (2)$$

The schematic for the SSB is shown on the right in Fig. 1. The main energy buffering capacitor C_1 is connected in series with a full-bridge converter. Capacitor C_1 instantaneously stores and releases the twice-line frequency energy with corresponding voltage ripple. Moreover, since v_{ab} is controlled with no dc-offset, the dc-bus voltage V_{out} appears completely on C_1. We can obtain the expression for the instantaneous voltage on C_1 to be

$$v_{C1} = \frac{\int i_{buf}\, dt}{C_1} = \Delta v_{C1} + V_{out} = \frac{-P_0}{2\omega V_{out} C_1} sin(2\omega t) + V_{out}, \quad (3)$$

For $v_{C1} + v_{ab}$ to equal the dc value V_{out}, the full bridge converter generates a terminal voltage v_{ab} that cancels the ripple voltage on C_1. The expression for v_{ab} is then

$$v_{ab} = -\Delta v_{C1} = \frac{P_0}{2\omega V_{out} C_1} sin(2\omega t). \quad (4)$$

Capacitor C_2 functions as the dc source of the full bridge converter. The dc value of v_{C2} must be regulated to sufficient voltage levels to generate the correct v_{ab} at any load. If not regulated, v_{C2} will gradually decay because of the loss in the full bridge converter. Control schemes in [4], [11] regulate v_{C2} by scaling a voltage term that is in-phase with i_{buf} to draw real power into the buffer converter and compensate for the converter loss. The voltage on C_2 is expressed as

$$v_{C2} = \sqrt{V_{C2,\,dc}^2 - \frac{I_{dc}^2}{8\omega^2 C_1 C_2} cos(4\omega t)} \quad (5)$$

The exemplar voltage waveforms of v_{C1}, v_{ab}, v_{C2} and v_{bus} in normal operation are plotted in Fig. 4.

As can be observed from the voltage and current expressions in (3), (4) and (5), the voltage and current stress in the full-bridge converter is heavily related to C_1, C_2 and the control of $V_{C2,\,dc}$, which implies an inherent trade-off between loss and volume. The multi-objective optimization scheme proposed in [10] quantifies the trade-offs and identifies the loss-volume pareto front. The SSB hardware designed in this work is designed with the optimization method, and has achieved 15% improvement in power density with higher efficiency than the previous hardware demonstrations [4], [5].

III. System Control

A. PFC Control

The control block diagram for the FCML boost PFC is shown on the left of Fig. 5. A PFC control scheme for boost converter operating in continuous conduction mode (CCM), similar to the classical multi-loop control [13], [14] is designed and implemented.

An inner current loop regulates the inductor current i_L to follow a desired current reference i_{ref} generated in phase with v_{rec}. To precisely match the phase of the input current to the input voltage and reject disturbance due to measurement noise, a phase-locked loop (PLL) based on a digital notch filter [15] is adopted in this design. Due to the small filter inductor in the FCML boost converter, the disturbance from the input voltage on the current is more significant than in conventional two-level boost converters with large filter inductors, which leads to problems such as current phase leading at line frequency. For this reason, a partial voltage feedforward control term is also included to offset such disturbance [8], [16].

The outer voltage loop regulates the output voltage to the desired dc value (i.e., 400 V) by scaling the magnitude of the input current. As shown in Fig. 5, the output voltage loop provides a multiplying factor k to the current loop reference.

B. SSB Control

To ensure normal operation, the SSB controller must fulfill two major functions: generating correct voltage to cancel the 120 Hz ripple on C_1 (annotated as "primary control" in Fig. 5) and drawing real power into the converter to regulate the dc voltage of v_{C2} (annotated as "compensate v_{C2}" in Fig. 5).

In [4], [11], these two functions are realized based on band-pass filter in the controller to extract the ripple component on

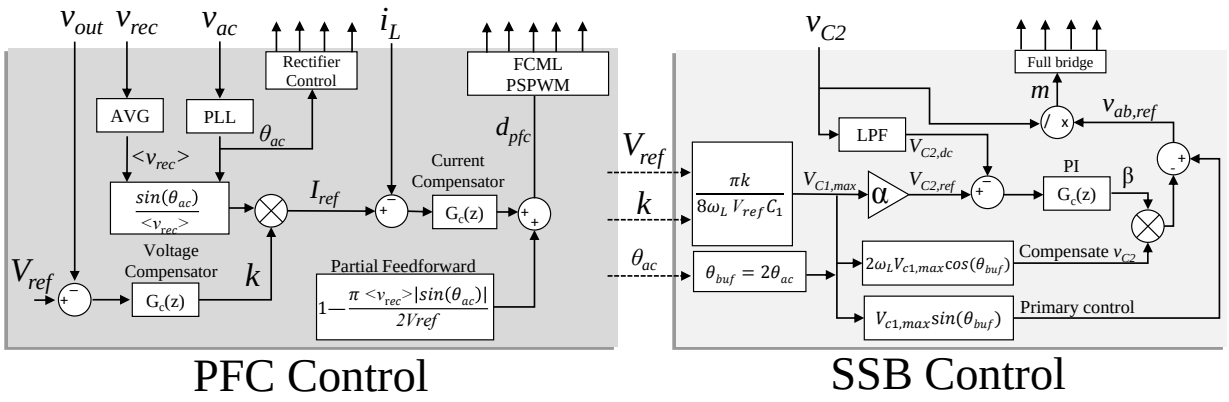

Fig. 5: Control diagram for the entire system.

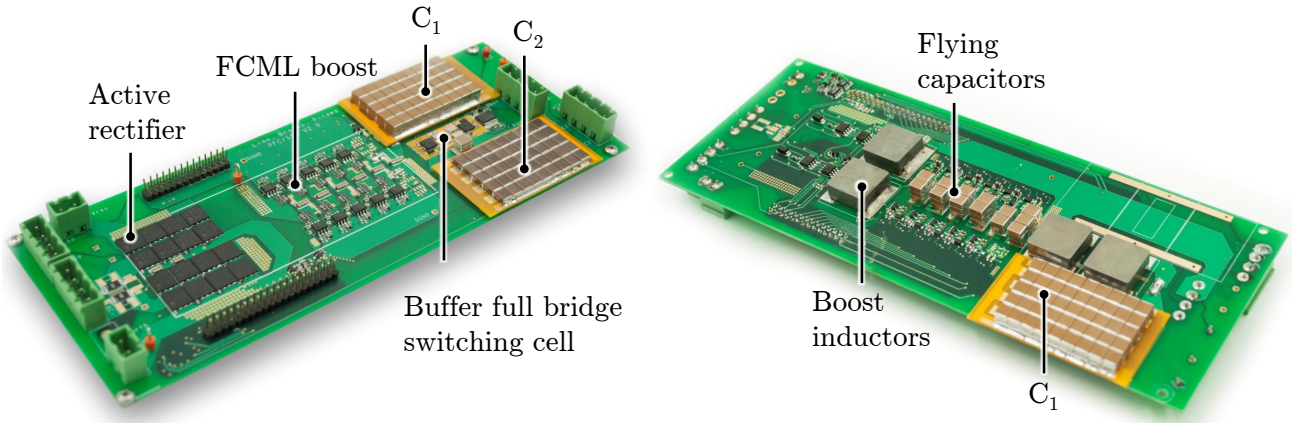

Fig. 6: Converter photos with key components annotated.

TABLE I: Component Listing of the Hardware Prototype

Function block	Component	Mfr. & Part number	Parameters
6-level FCML	GaN FETs	GaN Systems GS61004T	100 V, 15 mΩ
	Single flying capacitor	TDK C5750X6S2W225K250KA × 6	450 V, 2.2 μF
	Inductors (L)	Vishay IHLP6767GZER220M01 × 2	23 A, 22 μH
Series Stacked Buffer	GaN FETs	EPC 2033	150 V, 7 mΩ
	Capacitor C_1	TDK C5750X6S2W225K250KA × 180	450 V, 2.2 μF (0.431 μF @ 400 V)
	Capacitor C_2	TDK CGA9P3X7S2A156M250KB × 45	100 V, 15 μF (3.44 μF @ 80 V)
	Inductor	Vishay IHLP6767GZER470M11 × 2	8.6 A, 47 μH
Active rectifier	MOSFETs	STMicroelectronics STL57N65M5 × 4	650 V, 61 mΩ

C_1. However, because of high-order harmonics in the input current and low control bandwidth on the dc output voltage, band-pass filter based control suffers from noise on the dc bus. To solve this issue, the proposed control scheme utilizes three terms from the PFC controller – dc output reference voltage V_{ref}, voltage loop multiplying factor k, and angle of the input voltage θ_{ac} from the PFC PLL's output, to minimize the disturbance from the dc bus voltage.

If the input voltage is defined as $v_{\text{ac}} = V_{\text{ac}} sin(\omega t) = V_{\text{ac}} sin(\theta_{\text{ac}})$, the relation between the angle of v_{ab} (defined as θ_{buf}) and θ_{ac} can be determined from (4) as

$$\theta_{\text{buf}} = 2\omega t = 2\theta_{\text{ac}}. \tag{6}$$

(4) also indicates that the magnitude of Δv_{C1} (defined as $\Delta V_{\text{C1, max}}$) varies with the power level P_0. The voltage-loop factor k determines the magnitude of the input current reference I_{ref}. In a universal ac input PFC controller as in Fig. 5, the relation between k and I_{ref} is

$$I_{\text{ref}} = \frac{|sin(\theta_{\text{ac}})|}{< v_{\text{rec}} >} k = I_{\text{ac}} |sin(\theta_{\text{ac}})| \tag{7}$$

where $< v_{\text{rec}} >$ is the 120 Hz cycle average of the rectified input voltage. The relation between the magnitude of the input ac voltge V_{ac} and $< v_{\text{rec}} >$ is

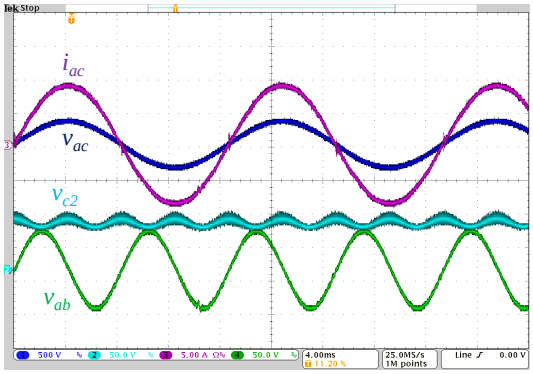

Fig. 7: Experimental waveforms of input voltage v_{ac}, input current i_{ac}, C_2 voltage v_{c2} and buffer converter output voltage v_{ab}. 240 Vac to 400 Vdc, 1.5 kW load.

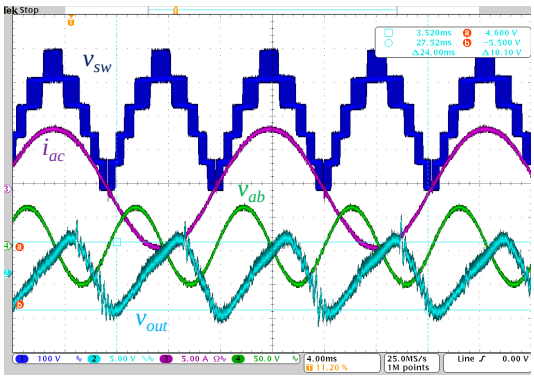

Fig. 8: Experimental waveforms of output dc voltage v_{out}, input current i_{ac}, switching node voltage v_{sw}, buffer converter output voltage v_{ab}. The output dc bus voltage is ac-coupled to show the ripple component. 240 Vac to 400 Vdc, 1.5 kW load.

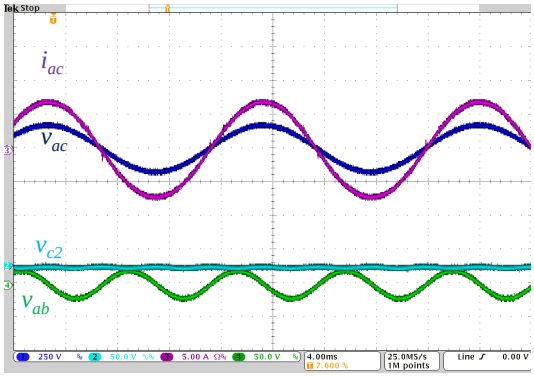

Fig. 9: Experimental waveforms of input voltage v_{ac}, input current i_{ac}, C_2 voltage v_{c2} and buffer converter output voltage v_{ab}. 120 Vac to 400 Vdc, 600 W load.

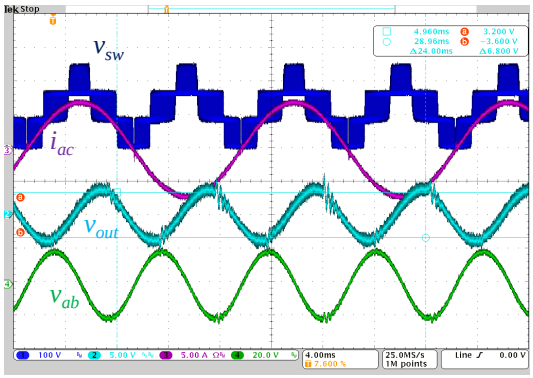

Fig. 10: Experimental waveforms of output dc voltage v_{out}, input current i_{ac}, switching node voltage v_{sw}, buffer converter output voltage v_{ab}. The output dc bus voltage is ac-coupled to show the ripple component. 120 Vac to 400 Vdc, 600 W load.

$$< v_{\text{rec}} >= \frac{2V_{\text{ac}}}{\pi}. \tag{8}$$

From (7) and (8), the relation between scaler k and rated output power P_0 can be derived as

$$k = I_{\text{ac}} < v_{\text{rec}} >= I_{\text{ac}} \frac{2V_{\text{ac}}}{\pi} = \frac{4P_0}{\pi} \tag{9}$$

which can be used to calculate $\Delta V_{\text{C1, max}}$ as

$$\Delta V_{\text{C1, max}} = \frac{\pi k}{8\omega V_{\text{ref}} C_1}. \tag{10}$$

Once the relative phase and magnitude of v_{ab} are obtained, a clean 120 Hz voltage reference signal and its derivative term for loss compensation can be generated with the built-in trigonometric Look-up Table (LUT) functions of the micro-controller (Texas Instrument C2000). Compared to the control schemes in [4], [11], the use of the LUT guarantees that only the 120 Hz component and no other harmonics is included in the generated v_{ab}. The derivative term for loss compensation does not need to be calculated from a digital differentiator as in [11]. Instead, it is generated with the LUT *cosine* function, which is much faster to compute. The reference voltage for $V_{\text{C2, dc}}$ is scaled with $V_{\text{C1,max}}$ to minimize voltage stress in the full-bridge at any load. The constraint for the scaler α is discussed in [9], [10]. Moreover, the proposed control scheme only needs to measure v_{C2}, which greatly simplifies sensing circuitry and reduces measurement noise. As a result, in practical software implementation in the micro-controller, the proposed control method greatly reduces the execution time of the control subroutine, which allows the potential to operate the converter with higher frequency and implement more safety and start-up control functions if desired. Detailed analysis on the characterization of SSB impedance, interaction with the PFC controls, and more comparison among different SSB control methods are discussed in [17].

IV. Hardware Prototype

A hardware prototype with the proposed architecture and control is designed and implemented on one main power board, as annotated in Fig. 6. The micro-controller is stacked on top of the power board. For the 400 V dc-bus considered here, each switch needs to block 80 V ($\frac{V_{\text{out}}}{5}$), so 100 V rated GaN FETs are used. The full bridge in the SSB is implemented on a separate PCB switching cell and soldered onto the main power board. Such switching cell design facilitates manufac-

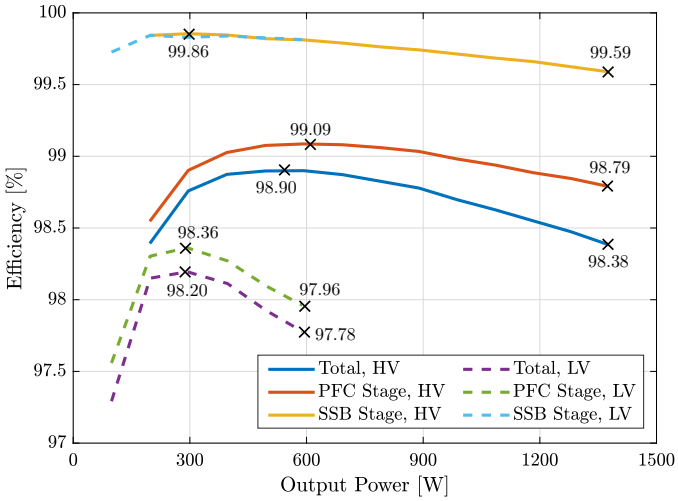

Fig. 11: Efficiency measurement with 240 Vac and 120 Vac input. Total system efficiency, PFC efficiency and SSB efficiency are plotted.

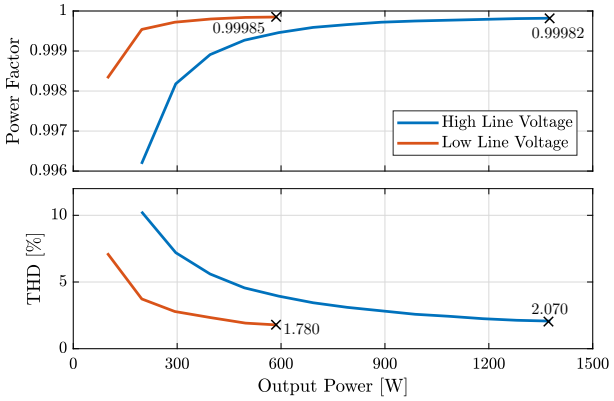

Fig. 12: Power factor and THD measurement for 240 Vac and 120 Vac input.

turing, repairing and debugging process [5]. Key components with their parameters are listed in Table. I.

V. Experimental Verification

The converter was tested with 240 Vac input up to 1.5 kW, and 120 Vac input up to 600 W (due to the current limit of the ac supply). Figure 7 and Fig. 8 show the operation at 1.5 kW, 240 Vac, and Fig. 9 and Fig. 10 show the operation at 600 W, 120 Vac. As can be seen in both test conditions, the input voltage and current are well in-phase, and the switching node voltage indicates good balancing among flying capacitors. Specifically, compared to the switch node waveform of the 7-level in [8], the staircase waveform is much more uniformed without obvious voltage band caused by the imbalance among flying capacitor voltages. For the SSB, v_{C2} is regulated with steady dc levels. And as the dc output voltage is ac-coupled in Fig. 8 and Fig. 10 to show the ripple component, it can also be observed that the proposed system control scheme is able to determine the correct phase and magnitude of v_{ab} to cancel the large ripple on C_1. The remaining small bus voltage ripple is introduced by the loss compensation term, as the bus ripple and v_{ab} are 90° out of phase. As shown in Fig. 8, at 1.5 kW, the peak-to-peak ripple is 10.1 V, which is 2.5% of the bus voltage.

Loss and power factor data are recorded with digital power analyzers Yokogawa WT3000E. Overall loss and buffer loss are measured, and corresponding loss in the PFC stage can then be calculated. The individual efficiencies of the FCML PFC stage and the SSB are and are illustrated in Fig. 11 for both 240 Vac and 120 Vac input. At 240 Vac input, The PFC stage reaches a peack efficiency of 99.1%. And the SSB alone is able to achieve ultra-high efficiency of above 99.5% across the full load range, thanks to the partial power processing characteristic and variable minimal $V_{C2,dc}$ control . Consequently, the peak total system efficiency is 98.9%, and at 1.5 kW, the efficiency is at 98.4%.

The power factor is above 0.996 for all tested loads, owing to the partial feedforward control. The Total Harmonic Distortion (THD) data for both high line and low line is collected with digital power analyzer Keysight PA2201, and they are well below the regulation limits. Power factor and THD for both high and low line are plotted in Fig. 12.

VI. Conclusion

The proposed PFC architecture with FCML boost front-end and SSB can greatly reduce the passive component volume compared to conventional solutions. Thanks to the improved design and control techniques implemented in this design, the FCML boost front-end reaches a power density of 490 W/in^3, and the SSB reaches a power density of 567 W/in^3 by box volume. The system is also able to achieve excellent performance in THD, power factor and dc-bus ripple. Moreover, we have also demonstrated that the proposed system control scheme can be implemented in an efficient way with a single DSP micro-controller.

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