Analysis and Design of a High Power Density Flying-Capacitor Multilevel Boost Converter for High Step-up Conversion

Zitao Liao, *Student Member, IEEE*, Yutian Lei, and Robert C.N. Pilawa-Podgurski, *Member, IEEE*

***Abstract*—This work explores the use of the flying-capacitor multilevel (FCML) topology in high step-up conversion. Compared to the conventional two-level boost converter, the FCML topology utilizes high energy density capacitors to facilitate inductors with storing and transferring energy during the conversion process, which brings features such as lower voltage stress on the switches, reduced voltage stress on the inductor and high effective switching frequency at the switching node. As a result, the total volume of the passive components in the converter is greatly reduced, while maintaining high efficiency at high voltage gain. To demonstrate the potential high power density and high efficiency, a hardware prototype that converts 100 V to 1 kV with 820 W maximum output power is built. Such specifications require careful optimizations in many aspects of the converter to ensure a high power density and efficiency design. The implemented solutions and associate design process are presented in detail, with comparison with other state-of-the-art solutions. The hardware prototype has successfully demonstrated a peak efficiency of 94.1%, and 329 W/in^3 (20 W/cm^3) overall power density.**

***Index Terms*—high step-up converter, flying-capacitor multilevel, high voltage, GaN.**

I. Introduction

High step-up DC/DC converters provide high voltage DC output in applications such as photovoltaic grid-connected power systems [1], large offshore wind farms [2] [3], medical power electronics such as X-ray power generator [4], satellite ion trusters [5], and pulse electric field (PEF) related applications [6] [7]. In these applications, high step-up converters are usually required to generate DC voltage at kilovolt levels from sources at hundreds of volts, with rated power ranging from hundreds of watts to few kilowatts. The conventional boost converter has many limitations with regard to achieving high voltage gain with high power density and efficiency simultaneously. Some of the major limitations are high voltage stress on switches and diodes, high conduction and switching losses [8], and large magnetic volume due to the low frequency switching of the required high voltage switches [2]. In [8], other non-isolated high step-up converter topologies and control methods that aim to solve such limitations are reviewed, including zero-voltage switching (ZVS) and zero-current switching (ZCS) to reduce switching loss, cascaded and interleaved designs to increase boost ratio and power rating, and multilevel designs to reduce switch voltage stress. However, many of these techniques incur trade-offs with other aspects of the designs. ZVS and ZCS converters usually require higher component rating, owing to the sinusoidal voltage or current waveforms [9]. Additionally, full ZVS or ZCS over the entire line and load range is difficult to achieve. Cascaded design increases voltage gain since it reduces the voltage gain requirement and eases the design for each individual stage, but the power density and efficiency of the combined converter is generally lower, owing to the combined size and power loss penalty [10]–[12]. The switched-capacitor (SC) converter is another type of converter that can achieve large step-up ratios. It utilizes the high energy density of capacitors [13] to transfer energy, resulting in much higher power density than conventional switched-inductor DC-DC buck or boost converters. However, SC converters have their own issues such as charge redistribution loss and no ability for lossless output load regulation [14], therefore their usage has mainly been in low power applications.

Hybrid inductive/capacitive converters are combinations of SC converters and conventional switched-inductor converters. They can achieve high power density by utilizing the high energy density of capacitors, while still allowing lossless load regulation and eliminating the charge redistribution loss in SC converters thanks to the extra inductors [11], [15], [16]. Intermediate voltage levels can be created by switching the capacitors in different configurations, thus some hybrid converters are also referred to as multilevel converters. The multilevel design allows lower voltage rating switching devices to be used for high voltage applications. Among the multilevel and hybrid converter topologies, the flying-capacitor multilevel (FCML) converter topology [17] has been demonstrated to achieve high power density and efficiency [18], [19], constructed with low voltage switches and smaller passive devices. While this topology has been investigated for use in step-up applications recently [20] (3-level), operation with large step-up (conversion ratio higher than 5) and higher frequency (i.e. higher than tens of kHz) has not been demonstrated.

In this work, the use of the FCML converter in high voltage step-up operation has been explored. A hardware prototype is implemented, converting 100 V to 1000 V with 820 W maximum output power and 94.1% peak efficiency. Comparing to state-of-the-art solutions, the proposed converter has demonstrated a significant improvement on the power density and efficiency, thanks to the inherent advantages of the FCML topology that allow the use of smaller inductors, low voltage switches and high energy density capacitors in the

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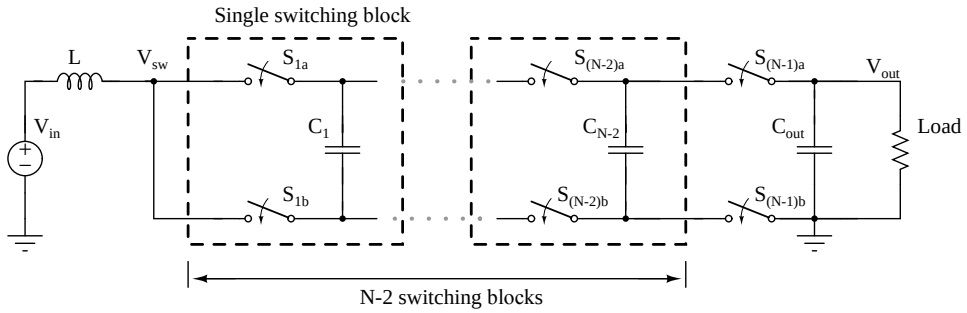

Fig. 1: Schematic of a N-level FCML boost converter.

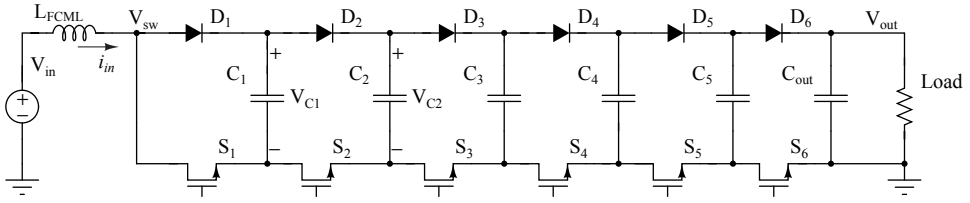

Fig. 2: Schematic of a 7-level FCML boost converter.

design. However, the high step-up scenario imposes challenges such as high switching loss, high degradation of capacitance and potential large voltage imbalance among flying capacitors, etc. Here we identify some of the key challenges for achieving compact and efficient high step-up with the FCML topology and present the corresponding solutions. In particular, an in-depth analysis on the reverse recovery loss for this type of converter is given, and an effective solution to reduce such loss is developed to improve the efficiency upon the work in [21]. More detailed analysis on the circuit operation such as charging/discharging cycle of the flying capacitors, practical switch rating considerations, and Discontinuous Conduction Mode (DCM) of the FCML converter are also included, for a more comprehensive discussion on the fundamentals of the FCML boost topology.

The remainder of this paper is organized as follows: Section II introduces the theory of operation of FCML converters and identifies critical equations as design guidelines. The practical challenges in the hardware design are also addressed with implemented solutions given in detail. Section III presents and analyzes the experimental results, and discusses proper modeling of the converter loss and potential methods to improve the efficiency. Section IV compares this work with state-of-the-art solutions for compact and efficient high step-up converters in the literature. Finally, Section V concludes the paper.

II. Proposed Solution for High Step-up Conversion

A. Principle of Operation

The schematic drawing of a generic, N-level FCML converter is shown in Fig. 1. As can be seen, it has $(N-2)$ switching blocks, each of which contains two switches and a flying capacitor. In total, a N-level FCML will have $(N-2)$ flying capacitors and $2(N-1)$ switches. The switches are controlled with phase shifted pulse width modulation (PSPWM) [17], [22]. Each switch is controlled by a pulse width modulation (PWM) signal with a duty ratio of D, and is phase-shifted by $\frac{360^\circ}{N-1}$ from the adjacent PWM signals. In steady state operation, the N-level FCML boost converter naturally balances the voltages across $(N-2)$ flying capacitors, each of which holds voltage of $\frac{V_{\text{out}}}{N-1}$, $\frac{2V_{\text{out}}}{N-1}$, ..., $\frac{(N-2)V_{\text{out}}}{N-1}$ [17], [23]. For example, in the 7-level FCML converter shown in Fig. 2, C_1 has a voltage of $\frac{V_{\text{out}}}{6}$, C_2 has a voltage of $\frac{2V_{\text{out}}}{6}$, etc.

Example PSPWM switching patterns of the converter are illustrated in Fig. 3 with a duty ratio of 0.9 and 60° phase shift for a 7-level FCML converter. To understand the energy transfer process among capacitors, let us start with the shaded time frames (a) and (b) in Fig. 3 and Fig. 4, and the corresponding circuit states with the current flow paths indicated in Fig. 5. During the time frame (a), S_1 is open while the remaining switches are closed, resulting in the switching node (labeled V_{sw} in Fig. 2) connecting to C_1. In this state, the inductor current is charging C_1 as shown in Fig. 5a. The voltage on C_1 starts to rise as shown in Fig. 4 (in this plot, voltages of C_1 and C_2 are normalized by $\frac{V_{\text{out}}}{6}$). Using the average inductor current I_{in}, the voltage ripple $\Delta V_{C_{\text{C1}}}$ on C_1 can be calculated by (1), which is also shown in Fig. 4. For the case of equal capacitance of flying capacitors considered here, each flying capacitor (C_{fly}) will then experience a corresponding voltage ripple $\Delta V_{C_{\text{fly}}}$, as given in (2). Thus, (2) can be used to calculate a desired capacitance for the worst case load current and duty cycle. At the end of this time frame (shaded area (a) in Fig. 3 and Fig. 4), the maximum voltage stress seen by the switch S_1 is as given in (3). It should be noted here that the transistor selection (voltage rating) is dependent on the flying capacitor voltage ripple (and thus the physical capacitance). During the time between (a) and (b), all the low-side switches are on, so switching node is connected to the ground. In the shaded area (b) in Fig. 3 and Fig. 4, S_2 is open while the remaining switches are closed as shown in Fig. 5b. The switching node voltage V_{sw} equals the voltage of C_2 minus the voltage of C_1,

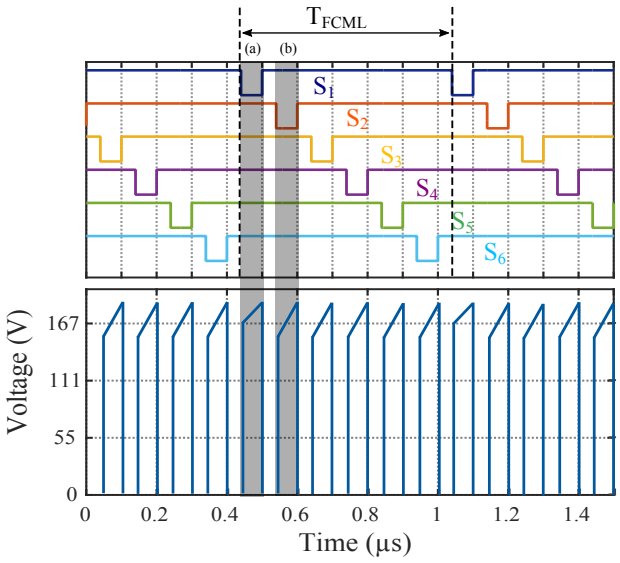

Fig. 3: Example simulated PSPWM signals with duty ratio of 0.9 (top) and the corresponding switching node voltage V_{sw} (bottom) from a 7-level FCML converter.

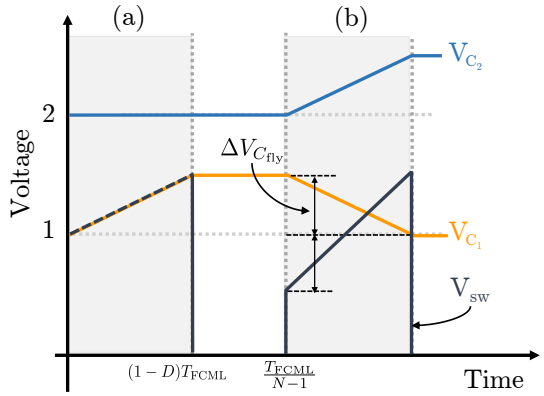

Fig. 4: C_1 and C_2 voltage waveforms with the resultant switching node voltage (voltages are normalized by $\frac{V_{\text{out}}}{6}$. The ratio of voltage ripples are enlarged for illustration purposes.)

yielding a switching node voltage of $\frac{V_{\text{out}}}{6} - \Delta V_{C_{\text{fly}}}$. At the end of the shaded area (b) in Fig. 4, C_1 is discharged back to the nominal voltage $\frac{V_{\text{out}}}{6}$, and the voltage of C_2 rises by $\Delta V_{C_{\text{fly}}}$, while the switching node voltage rises to $\frac{V_{\text{out}}}{6} + \Delta V_{C_{\text{fly}}}$.

$$\Delta V_{C_{\text{C1}}} = \frac{I_{\text{in}} T_{\text{FCML}}(1-D)}{C_1} \tag{1}$$

$$\Delta V_{C_{\text{fly}}} = \frac{I_{\text{in}} T_{\text{FCML}}(1-D)}{C_{\text{fly}}} \tag{2}$$

$$V_{\text{switch}} = \frac{V_{\text{out}}}{N-1} + \Delta V_{C_{\text{fly}}} \tag{3}$$

This charging and discharging process continues among adjacent flying capacitors, utilizing both the inductor and capacitors to transfer energy to the load. It also creates the frequency multiplication effect on the switching node seen by the inductor in the FCML converter. In Fig. 4, the corresponding switching node voltage is switched between 0 V and $\frac{V_{\text{out}}}{N-1}$ (with voltage ripple) in $\frac{T_{\text{FCML}}}{N-1}$ of the time, which means the equivalent frequency of the switching node voltage is $(N-1)$ times (six times in this case) of the switching frequency of any individual switch. The switching node voltage waveform of a 7-level FCML converter in one switching period can be seen at the bottom of Fig. 3, which shows simulated (LTSPICE) waveforms. With such switching node waveform on the inductor L, the equation for the required input inductance of the FCML boost converter can be written as (4), in terms of desired operation parameters: Switching duty ratio D, V_{in}, number of levels in the FCML N, transistor switching frequency f_{FCML}, and allowed inductor current ripple ΔI_L.

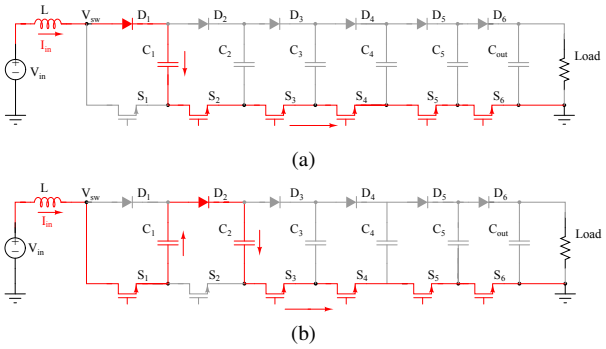

Fig. 5: Current path when S_1 is open (top) during time frame (a) and S_2 is open (bottom) during time frame (b).

$$L_{\text{FCML}} = \frac{V_{\text{in}}(1-(1-D)(N-1))}{\Delta I_L f_{\text{FCML}}(N-1)}. \tag{4}$$

$$L_{\text{boost}} = \frac{V_{\text{in}} D}{\Delta I_L f_{\text{sw}}} \tag{5}$$

Notice that if $N = 2$, (4) can be simplified to (5), which is the inductance constraint in a conventional boost converter. In other words, the conventional boost converter can be viewed as a two-level FCML converter. Inserting $N = 7$ for the proposed converter and $N = 2$ for a conventional boost converter into (4), the inductor size of the FCML converter is calculated to be 13.5 times smaller than that of the conventional boost converter, given the same input power, conversion ratio and current ripple requirements.

Comparing the form of (4) and (5), this dramatic reduction of the inductor size can be seen as the result of two effects [24]. The first one is the change of equivalent duty ratio of the switching node voltage. In (5), the duty ratio of the switching node voltage is the same as the duty ratio D of the switches. In (4), the effective duty ratio of the switching node voltage seen by the inductor is reduced to $(1-(1-D)(N-1))$. The second effect is the frequency multiplication as discussed earlier that the effective frequency at the switching node is $f_{\text{FCML}}(N-1)$.

Volt-second balance condition on the inductor L_{FCML} in (6) can be applied to find the average conversion ratio, where the left-hand side is the volt-second on the inductor when $V_{\text{sw}} = \frac{V_{\text{out}}}{N-1}$, and the right-hand side is the volt-second when switching node is connected to the ground. By simplifying (6), the

overall voltage conversion ratio of the FCML boost converter in Continuous-Conduction Mode (CCM) can be simplified to found as (7). Notice that this voltage conversion relation is the same as a regular boost converter. The condition in (8) is derived as the constraint for CCM operation, which ensures the ratio between the current ripple and the average input current to be less than or equal to two. If such condition is not met, the converter will operate in Discontinuous Conduction Mode (DCM), where the conversion ratio will be different, as shown in (9). The detailed derivation of (8) and (9) are given in the appendix.

$$(\frac{V_{\text{out}}}{N-1} - V_{\text{in}})(1-D)T_{\text{FCML}} = V_{\text{in}}(\frac{1}{N-1} - (1-D))T_{\text{FCML}} \tag{6}$$

$$V_{\text{out}} = \frac{V_{\text{in}}}{1-D} \tag{7}$$

$$L_{\text{FCML}} f_{\text{FCML}} \geqslant 0.5(1-D)^2(D - \frac{N-2}{N-1})R_{\text{out}}, D \geqslant \frac{N-2}{N-1} \tag{8}$$

$$V_{\text{out}} = V_{\text{in}}(\frac{N-1}{2} + \frac{\sqrt{(N-1)^2 + 2(N-1)(D-\frac{N-2}{N-1})^2 \frac{T_{\text{FCML}} R_{\text{out}}}{L_{\text{FCML}}}}}{2}), D \geqslant \frac{N-2}{N-1} \tag{9}$$

B. Hardware Implementation

A 7-level FCML boost converter prototype with specifications shown in Table I has been built to demonstrate the potential of FCML converters to achieve high power density and efficiency for high step-up conversion applications.

Thanks to the reduced voltage rating for individual switches in the FCML topology, 200 V GaN switches and diodes are used, which allows lower $R_{\text{ds, on}}$ and lower forward drop, respectively, for lower conduction loss. Moreover, compared to high voltage MOSFET or SiC switches, lower voltage rating GaN switches reduce switching loss because of the smaller output capacitance and fast switching performance. The use of diodes instead of GaN transistors for the top six switches in Fig. 2 is deliberate. This is because at the high duty ratio (0.9) used in this high step-up application, the diodes only conduct for one tenth of a switching period. Thus, while the diodes are generally less efficient than the GaN switches (owing to the relatively large conduction loss from their forward voltage drop), the power processed by the diodes is far smaller. Moreover, with the proposed method to reduce the loss from reverse recovery effect, the full converter can achieve a comparable efficiency to the synchronous configurations, while the circuitry required to drive an active switch in FCML converter (such as gate drivers, signal and power level-shifters) are saved. Thus there is considerable saving in Printed Circuit Board (PCB) size and component cost while the penalty in efficiency due to the use of diodes is minimal, for the high step-up scenario considered here.

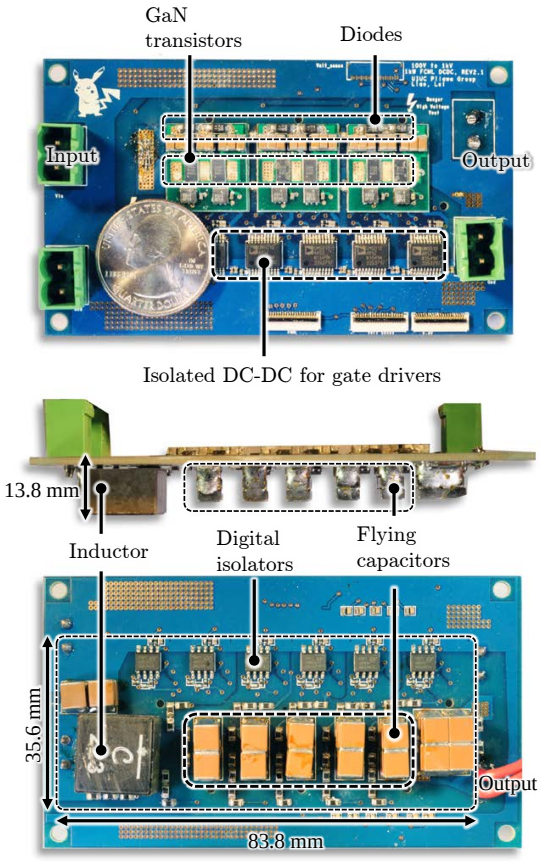

Fig. 6: Annotated photographs of the prototype PCB with US quarter.

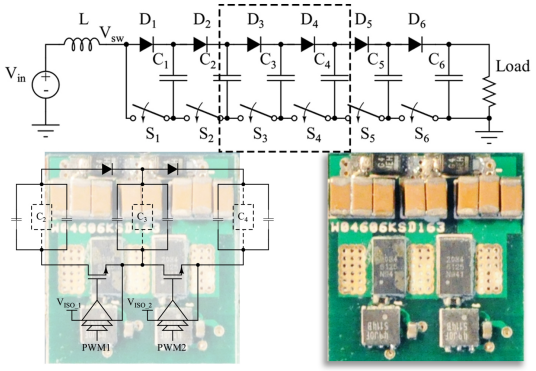

Fig. 7: Switching cell schematic and PCB.

The top, side and bottom views of the prototype converter are shown in Fig. 6, with key components annotated and a US quarter for size comparison. The flying capacitors and inductors are placed on the bottom side of the PCB. GaN switches and diodes are placed on a custom switching cell (shown in green) that incorporates two gate drivers and local decoupling capacitors to minimize ringing at switch transitions. The dimension of the rectangular cuboid enclosure (L $\times$ W $\times$ H) that only contains switches and passive components is 3.3 in $\times$ 0.67 in $\times$ 0.54 in (83.8 mm $\times$ 17.0 mm $\times$ 13.716 mm), which is used to calculate the power stage power density. The dimension of the rectangular cuboid (L $\times$ W $\times$ H) which

TABLE I: Specifications of the 7-level FCML boost converter prototype.

Rated power	820 W
Input voltage	100 V
Maximum output voltage	1 kV
Transistor switching frequency	72 kHz

TABLE II: Component list of the converter PCB.

Component	Part number	Parameters
GaN transistor (S_1 to S_6)	EPC 2034	200 V, 31 A, 10 mΩ
GaN gate driver	Texas Instruments LM5114	
Diodes (D_1 to D_6)	Vishay VS2EFH02	200 V, 2A
Flying capacitors ($C_1 - C_5$)	TDK C5750X6S2W225K250KA ×6	2.2 μF, 450 V
Inductor	Coilcraft XAL1510-223	22 μH
Digital isolators	Silicon Labs Si8423BB-D-IS	
Power isolators	Analog Devices ADUM5210	

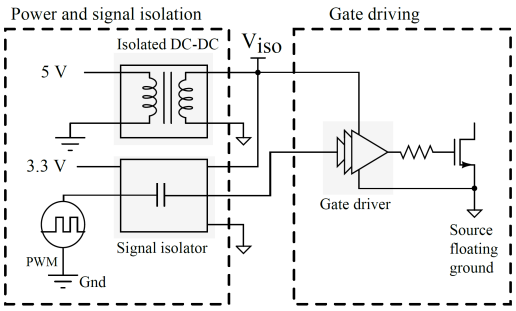

Fig. 8: Gate driving power and signal isolation circuits for each GaN FET.

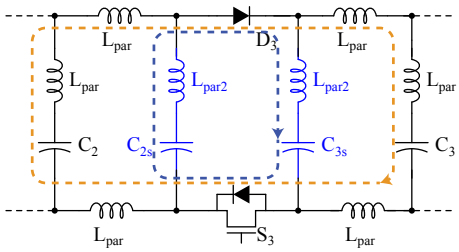

Fig. 9: Original commutation loop (yellow) and added decoupling paths (blue).

includes the power stage and all the level shifting circuits is 3.3 in × 1.4 in × 0.54 in (83.8 mm × 35.6 mm × 13.716 mm), which is used to calculate the overall power density of the converter.

1) Gate driving circuitry and switching cells: A detailed schematic drawing and a photo of the switching cell PCB are presented in Fig. 7. Since the source node of each GaN FET is floating, the PSPWM signals from the microcontroller unit (MCU) need to be isolated. Figure 8 shows the complete gate driving power and signal isolation circuit. The 5 V grounded power is shifted with the on-chip isolated DC-DC converters ADUM5210 as denoted in Fig. 6. The PSPWM signals are isolated with RF-based signal isolator Si8423BB-D-IS on the bottom side of the main PCB. This circuit ensures the complete isolation between low voltage low power control circuit (MCU and 5 V control power etc.) and the main power stage. Techniques in [25] to generate floating gate driving power supply voltages can further shrink the PCB area needed for the level-shifting circuits as well as improve the efficiency by eliminating the relatively lossy isolated DC-DC converters. For testing the converter in this work, the gate driving power was supplied by an external power source. However, such external power source can be replaced with the voltages from the flying capacitors themselves by carefully controlling the start-up sequence and flying capacitor voltages [26].

The gate drivers, gate resistors, GaN switches and diodes are laid out in a compact fashion on the switching cell PCB to minimize the commutation loop and the gate driving loop to reduce the parasitic inductance in the PCB traces. Methods to further reduce the loop inductance in the FCML converter such as placing additional decoupling capacitors and different layout techniques are discussed in [18], [27] for other applications. The schematic in Fig. 9 shows the decoupling concept. C_2 and C_3 are the flying capacitors as shown in Fig. 6, and C_{2s} and C_{3s} are the small decoupling capacitors on the switching cell PCB in Fig. 7. With the decoupling path shown in blue, the influences from the large parasitic inductances in the original commutation loop shown in yellow is minimized.

These efforts have enabled a GaN-based 7-level structure without large voltage overshoot during switching, something that to date have impeded the development of high (i.e. $\geqslant 5$) level FCML boost converters with high switching frequencies. Moreover, since this converter relies on the natural balancing properties of the FCML topology, this symmetrical board layout also helps minimize the parasitic effects that will cause unbalanced charge/discharge cycles on flying capacitors that in turn lead to voltage imbalance among flying capacitors [28]. Imbalanced capacitor voltages increase the drain-source voltage, which can lead to switch failure if the blocking voltage exceeds the switch rating. This modular construction also facilitates the manufacturing and debugging process, where

the switching cells can be tested for functionality individually before being assembled onto the converter board and quickly replaced if switch failure occurs.

2) High voltage capacitor implementation: To achieve high power density and efficiency, ceramic capacitors are used in this converter since they have much higher energy density than film capacitors and much lower ESR and ESL than electrolytic capacitors [13]. One important design consideration is that with ceramic capacitors, the capacitance at full rated voltage can be reduced by a factor of 4 to 10, compared to the rated value at zero bias voltage [13]. This change in capacitance can affect the natural balancing of the flying capacitor voltages, as well as the voltage ripple on each flying capacitor. Imbalance of the flying capacitor voltages and large capacitor voltage ripple can lead to switch failure if the switch voltage exceeds the rating, so the reduction of effective capacitance with increasing voltage has to be taken into account at early design stage.

Since the target output voltage of the converter is 1 kV, the output capacitor should be rated for 1 kV. Correspondingly, the flying capacitors should be rate for $\frac{1000}{6}$ V, $\frac{2000}{6}$ V, ..., $\frac{5000}{6}$ V from C_1 to C_5. To meet the voltage requirement for C_{out} and C_5, a few design options to realize high voltage capacitors were considered.

The first option is to directly use 1 kV rated ceramic capacitors. One such example of ceramic capacitors with a reasonable energy density and physical size is the 0.47 uF capacitor from Knowles Syfer [29] with a footprint of standard 2220 (5750 metric) package and a height of 4.5 mm. However, the effective capacitance of this ceramic capacitor at 1000 V will degrade to one tenth of the nominal value, which results in an effective energy density of 0.183 mJ/mm^3. The second option is to construct a 1000 V capacitor using two 500 V rated ceramic capacitors with X6S dielectric material [30] connected in series. For this configuration, the capacitance only degrades to one fourth of its nominal value when operating at the full rated voltage. This results in an effective energy density of 0.78 mJ/mm^3, which is four times larger than using the 1000 V capacitor. Overall, the volume of a set of ceramic capacitors (say for C_5) is 427.5 mm^3 for an effective capacitance of 0.825 μF, by using a total of six of the 500 V capacitors as connected in Fig. 10. Even though the remaining flying capacitors from C_1 to C_4 require lower rated voltage, using lower voltage rating capacitors with smaller physical size for them will not decrease the dimensions of the rectangular cuboid that encloses the converter, as the maximum height is determined by the stacks of ceramic capacitors for C_5 and C_{out} as shown on the left of Fig. 10. In order to fully utilize the rectangular cuboid spaces, configuration in Fig. 10 was also implemented for C_1 to C_4. Including the inductor and the input capacitor, the total volume of the passive components is 5740 mm^3. It should be noted that for other scenarios or more optimized layout, the amount of ceramic capacitors to implement lower voltage flying capacitors could thus be reduced, if desired.

One challenge of this approach is the voltage balance between two capacitors connected in series. In the application considered here, series voltage imbalance is exacerbated by the combination of high-current and high-frequency charge and discharge cycles of the capacitors. Any voltage imbalance, if large enough, will cause voltage overstress and the eventual failure on one capacitor. To ensure equal voltage share, two balancing resistors are placed as shown in Fig. 10. The rated voltage and resistance of the balancing resistors must be chosen to simultaneously balance the capacitors and dissipate very low power. For the prototype, a resistance of 330 kΩ is found to be sufficient to balance the capacitors while only dissipating a maximum power of 0.6 W on each resistor.

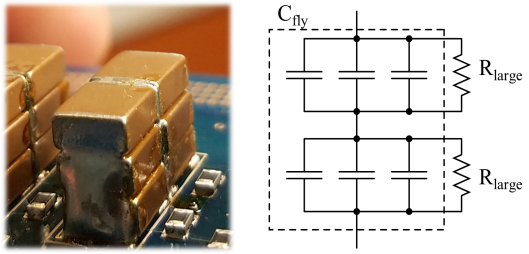

Fig. 10: Single flying capacitor implementation.

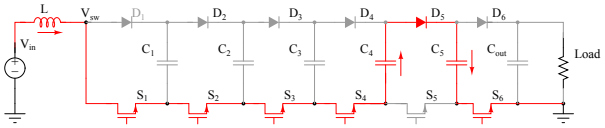

Fig. 11: C_4 and C_5 connected in series.

As discussed earlier, the effective capacitance of ceramic capacitors is degraded at higher voltage bias. If the same capacitor configuration is applied to all flying capacitors, the capacitors closer to the output will have lower effective capacitance than those closer to the input during the operation of the converter, which also leads to larger voltage ripple. For this reason, when C_4 and C_5 are connected in series with the inductor as shown in Fig. 11, the largest capacitor voltage ripple is expected, which will be seen by switch S_5. The voltage stress on S_5 at maximum input current of 8.2 A and maximum output voltage of 1 kV can be regarded as the minimum switch voltage rating. With 72 kHz switching frequency and an effective capacitance of 0.825 μF, the voltage rating is calculated to be 180.5 V by (2) and (3), allowing 200 V devices to be used in this design.

3) Diode selection: In hard-switched converters employing p-n diodes, one major source of switching loss comes from the reverse recovery effect of the p-n junctions [31]. The reverse recovery current will introduce extra losses on the switches and diodes themselves. Since the reverse recovery charge Q_{rr} and time t_{rr} increase with increasing diode current turn-off rate $\frac{di}{dt}$, the reverse recovery effect is expected to be an important loss mechanism due to the use of fast-switching GaN switches in this work.

The Schottky diode is known for having very little reverse recovery effect since it is a majority-carrier device. However, higher rating ($\geqslant$ 200 V) Schottky diodes will still produce large peak reverse recovery current because of the parallel guard-ring p-n junction diode [32]. As confirmed by [33] as well as our own measurement, the reverse recovery current is

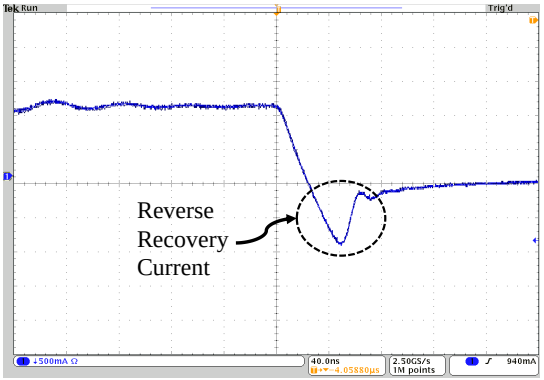

Fig. 12: S320 Schottky diode reverse recovery current (2 V to 20 V conversion, 1 A input current).

TABLE III: Selected Tested Diodes.

Part number	Parameters	Type
Fairchild S320	200 V, 3 A	General Purpose Schottky
Diodes PDS3200	200 V, 3 A	General Purpose Schottky
STMicro STPS2200	200 V, 2 A	Power Schottky
Diodes SBR10U	200 V, 10 A	Super Barrier
Vishay VS2EFH02	200 V, 2 A	Hyperfast Reverse Recovery

indeed found to be significant for 200 V Schottky diodes, as shown in the example converter waveform in Fig. 12. Another type of diode that is known for having very small reverse recovery behavior is the SiC diode [34]. SiC diodes usually have high ($\geq$ 600 V) blocking voltages, which means they have much larger on-resistance than lower voltage rated p-n diodes in general. The model that has been tested in this work is the 600 V, 3.3 A, C3D1P7060Q SiC diode from Cree. Experimental evaluation of these diodes showed that the RMS conduction loss due to large on-resistance was too high as a trade-off for low reverse recovery loss.

Most diode manufacturers provide limited information on the detailed reverse recovery characteristics, which makes it difficult to estimate the associated losses at various operating conditions. For this reason, various types of diodes rated for 200 V have been evaluated under identical conditions (30 V to 300 V conversion, 72 kHz switching frequency). Since the selected diodes have similar forward drops, their conduction losses are well matched. Under the same test conditions, the different switching losses can be extracted from the difference in overall converter losses when using different diodes. Some major types of diodes that have been tested are general purpose Schottky, power Schottky, hyperfast recovery and super barrier diodes. Since diodes of the same categories showed similar performance, selected test results of a few typical diodes of their categories are presented in Fig. 13 and tested diode specifications are listed in Table III.

It can be seen that the switching loss from the hyperfast reverse recovery diode is the lowest across the tested load range. A detailed loss breakdown based on the reverse recovery characteristics of the Vishay VS2EFH02 diode will be discussed in the next section.

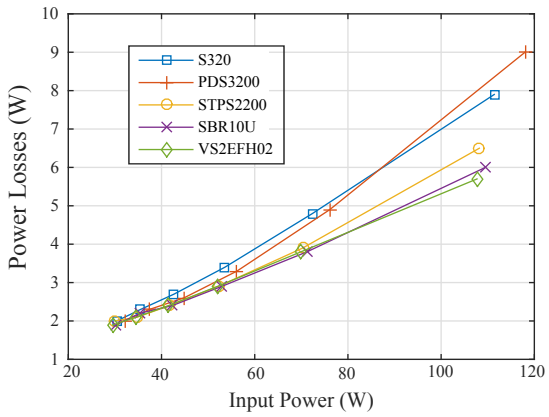

Fig. 13: Converter power losses with different diodes (30 V to 300 V conversion, 72 kHz switching frequency).

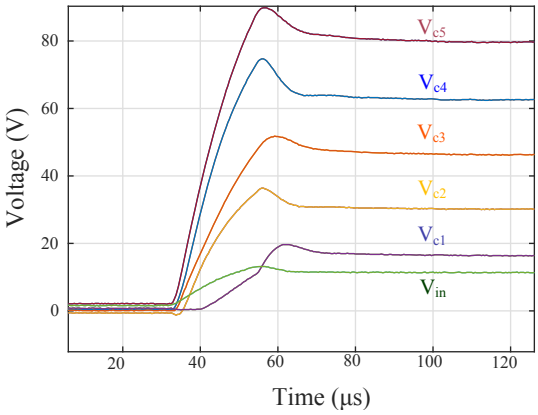

Fig. 14: Measured flying capacitor voltages during a input voltage transient from 0 V to 10 V.

III. Experimental Verification

The converter was tested with an input voltage of 100 V and operated with open-loop control with constant duty ratio of 0.9 to generate 1 kV output voltage. If strict load regulation on the output voltage is required, a voltage regulator can be designed based on the average model of the regular boost converter, as the average model for FCML is identical to the boost converter below the switching frequency [35]. Initially, the converter was constructed with six hyperfast diodes as shown in Fig. 2. Following this, several methods were explored to reduce reverse recovery loss. The final design of the converter achieved 100 V to 1 kV conversion with 820 W maximum output power and 94.1 % peak efficiency within the tested load range.

A. Natural balancing of flying capacitor voltages

The flying capacitor voltages are monitored with National Instrument data acquisition system (PXIe-1073). Initially, the behavior of the converter is verified at low power and low voltage in Fig. 14. Operation at low voltage enabled high precision capacitor voltage measurements to be performed, which was difficult to obtain from the high voltage experimental enclosure

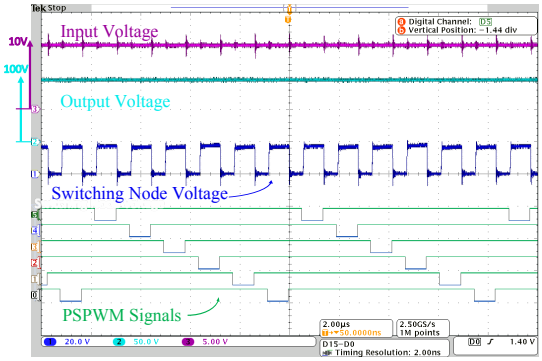

Fig. 15: Input, output and the switching node voltages with PWM signals (V_{in}= 10 V, V_{out} = 100 V, P_{out}= 20 W).

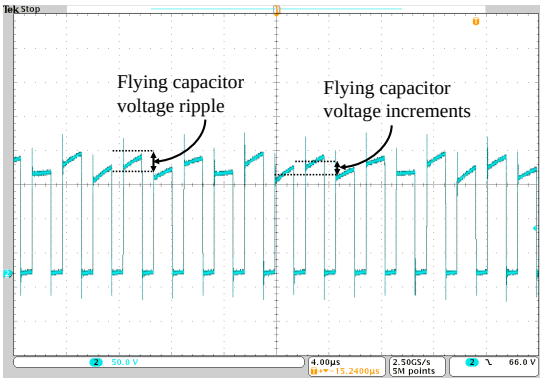

Fig. 16: Switching node voltage (V_{in}= 100 V, V_{out} = 914 V, P_{out}= 750 W).

during full power/voltage testing. Figure 14 shows the voltages of capacitors C_1 to C_5 and the input voltage during start-up with a 10 V input. It confirms that the flying capacitor voltages are in good balance as the voltages are around 16 V, or $\frac{V_{\text{out}}}{N-1}$, apart from each other. It should be noted that the overshoot in voltages is not due to the dynamics of the converter. It is caused by the fact that the input power supply has an overshoot at the end of a fast ramping, as can be observed from the trajectory of V_{in}.

Another way to evaluate the natural balancing performance is to monitor the switching node voltage V_{sw}. A converter with good natural balancing should have switching node voltage with even height pulses with $\frac{V_{\text{out}}}{N-1}$ peak voltage if the duty ratio is greater than $\frac{N-2}{N-1}$ (in this case, 0.9 is greater than $\frac{5}{6}$). Shown in Fig. 15 and Fig. 16 are measured switching node (V_{sw} of Fig. 4) voltages for V_{in} = 10 V and 100 V, respectively. It can be seen from the measured waveform in Fig. 16 that the pulses are not as even as in the simulated waveform in Fig. 3. These slight deviation from simulated flying capacitor voltages in the waveform is denoted as the voltage increment. The quantitative analysis performed in [28] showed that practical implementation concerns in the converter such as output capacitor voltage ripple, gate signal mismatches and other parasitics in the PCB and among others will cause voltage imbalance in FCML converters. As a result, in the 7-level FCML considerded here, the voltages on C_1, C_3 and C_5 tend to drift higher than the nominal balanced flying capacitor voltages, and the voltages on C_2 and C_4 stay very close to the ideal balanced voltages. This is the reason why only the adjacent pulses on the switching node voltage have uneven heights in Fig. 16. The natural balancing effect damps such voltage deviation with the series resistance in the circuit and stabilize the capacitor voltages to new steady-state values [23]. To maintain the voltage increments on flying capacitors within reasonable range with passive natural balancing mechanism, in this work, careful design of adequate output capacitors, symmetric and low inductance layout have been implemented to minimize the disturbances on flying capacitor voltages. Active balancing techniques can be implemented to further improve the balancing performance, but with extra cost of more complicated sensing circuitry and controller design [36]–[38].

B. Loss breakdown

The power loss can be categorized into five major sources: GaN FETs conduction loss, overlap switching loss, diode conduction loss, inductor loss, which includes both core loss and DCR conduction loss, and the extra switching loss introduced by diode reverse recovery effects. The first three categories can be calculated fairly accurately with the given information from the datasheets of the switching components. The inductor core loss can also be estimated from the loss model provided by the manufacturers.

Extra power loss introduced by the reverse recovery current can be estimated by multiplying the energy loss for every reverse recovery transition from (10) with the switching frequency [39], where Q_{rr} is the total reverse recovery charge, and t_{rr} is the reverse recovery time. However, since the values of Q_{rr} and t_{rr} not only change with the diode current turn-off rate $\frac{di}{dt}$, but also with the temperature, the exact loss can be difficult to calculate at different power levels as the temperature changes along. To reflect the effect of temperature on such loss, assumptions shown in Fig. 18 are made that the diode temperature rises linearly with the input current, and Q_{rr} and t_{rr} are also proportional to the temperature for a first-order estimation [40], [41]. The Q_{rr} v.s. $\frac{di}{dt}$ and t_{rr} v.s. $\frac{di}{dt}$ curves in Vishay VS2EFH02's datasheet [42] at different temperatures are extrapolated to determine the corresponding Q_{rr} and t_{rr} at different power levels. The current turn-off rate $\frac{di}{dt}$ is calculated with the average inductor current and the turn-on time of the GaN FETs.

$$E_{\text{rr}} = V_{\text{out}}(t_{\text{rr}} I_{\text{in}} + Q_{\text{rr}}) \tag{10}$$

C. Reduction of Reverse Recovery Loss

Even though effort has been made to reduce reverse recovery loss in the process of diode selection as discussed in Section IIB, the loss breakdown estimation in Fig. 17 still shows that reverse recovery loss is the largest portion of the total loss as power increases to a certain level, which brings up the discussion of how to alleviate such loss with other possible techniques.

One potential method to improve the efficiency is to apply Quasi Square Wave Zero Voltage Switching (QSW-ZVS)

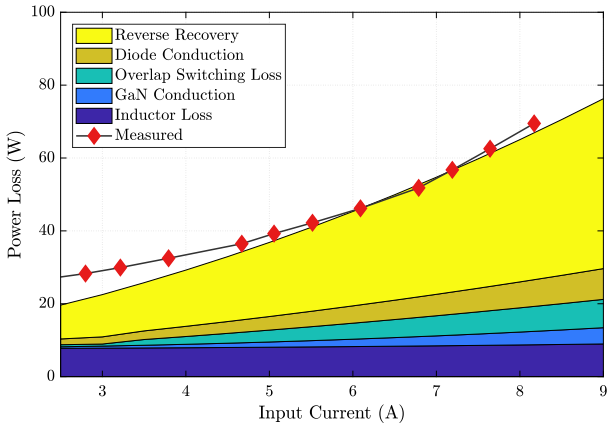

Fig. 17: Measured loss and loss breakdown for 100 V to 1 kV conversion.

Assumptions:

$$\left.\begin{aligned} Q_{\mathrm{rr}} &\propto T \\ t_{\mathrm{rr}} &\propto T \\ T &\propto I_{\mathrm{in}} \end{aligned}\right\} \xrightarrow{E_{\mathrm{rr}} = V_{\mathrm{out}}(t_{\mathrm{rr}} I_{\mathrm{in}} + Q_{\mathrm{rr}})} E_{\mathrm{rr}} \propto {I_{\mathrm{in}}}^2$$

Result:

Fig. 18: Assumptions for modeling the reverse recovery loss.

technique in [43] to lower the switching loss caused by diode's reverse recovery effect with zero-current turn-off on the diodes. QSW-ZVS is realized by operating the converter in shallow DCM or boundary-conduction mode. However, the large inductor current ripple in this case will increase the core loss and DCR loss on the inductor, as well as RMS conduction loss on GaN FETs and diodes, which introduces significant amount of loss as a trade-off to the reduced switching loss, especially at heavy load conditions. For this reason, this method requires careful optimization on the inductor to achieve the overall improvement on the converter efficiency, which will not be discussed in this paper.

Another method that has been implemented in [33] to alleviate this type of loss is to connect four lower voltage rating Schottky diodes in series to function as a single high voltage rating device. Since each of them has negligible reverse recovery effect because they have no guard-ring p-n diode as in the higher voltage rating Schottky diodes, this configuration will introduce minimum reverse recovery loss. However, this design will increase the total diode forward drop voltage loss and reduce the overall conversion ratio. It is also difficult to ensure that the voltage is shared equally among diodes when they are reverse-biased, and if it is not, possible damage could happen to the devices. The method that has been implemented in this work is to parallel-connect each diode with another diode as shown in Fig. 19. This method has been demonstrated to be very effective and manage to bring significant reduction of overall losses on the diodes. As shown in (10), the reverse recovery loss increases with the input current. Moreover, the values of Q_{rr} and t_{rr} both change with temperature (T), which varies with input current as well. With the assumptions in Fig. 18, the reverse recovery

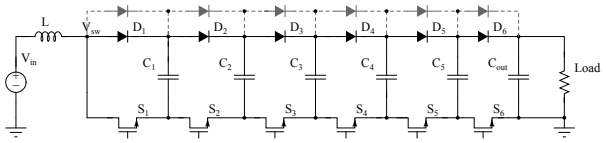

Fig. 19: Converter with extra parallel diodes.

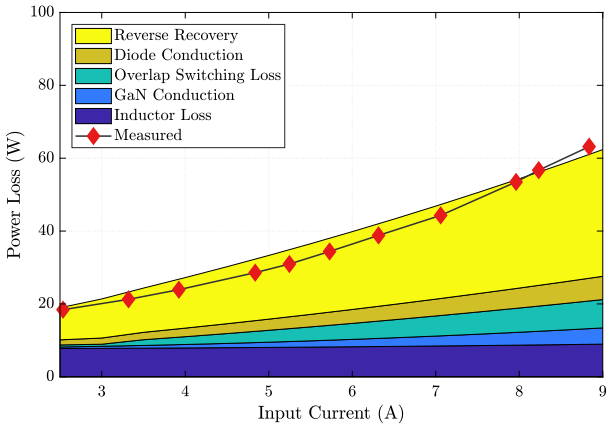

Fig. 20: Measured loss and loss breakdown for 100 V to 1 kV conversion with extra parallel diodes.

loss can be estimated to be proportional to the square of the input current, to the highest order. With two diodes sharing the current that used to be carried by one diode, the temperature of each diode will rise much slower as input current increases, which means at the same input current, the values of Q_{rr} and t_{rr} are much lower. The reverse recovery loss is expected to be reduced by nearly half because of the aforementioned assumed linearities.

One of the common-known problems for paralleling diodes is the thermal run-away effect caused by unequal sharing of current and temperature between diodes. If there is a mismatch of temperature between two diodes, the hotter diode will have lower forward drop voltage such that it will carry more current, and the difference in temperature will be enlarged. The end result is that one diode will carry most of the current and get much hotter than the other. To avoid the thermal run-away effect, all parallel-connected diode pairs are placed very close to each other on the PCB with copper traces underneath and heatsink on the top to ensure thermal equilibrium.

Figure 20 shows the calculated loss breakdown and the measured loss with two diodes in parallel for 100 V to 1 kV conversion from 2.5 A to 10 A input current. In comparison to the single diode case in Fig. 17, both the calculated loss from the loss model and the experiment results are approximately 10 W lower at 8 A input current with extra parallel-connected diodes, and the converter was able to achieve 94.1% peak efficiency across the full tested load range as shown in the efficiency plot of Fig. 21.

IV. Comparison with other high step-up converters

Compared to other works that have explored methods for compact and efficient step-up conversion in Table IV, this converter showed good balance among efficiency, power density

TABLE IV: Comparison of recent work on high step-up converters.

	[44]	[45]	[33]	This work
Rated power	450 W	250 W	2 kW	820 W
Input voltage	25-30 V	28-38 V	275 V	100 V
Max output voltage	400 V	300-980 V	2 kV	1 kV
Peak efficiency	96%	97%	84%	94.1%
Switching frequency	100 kHz	100 kHz	13.56 MHz	72 kHz
Overall power density	38 W/in^3	19 W/in^3	250 W/in^3	329 W/in^3

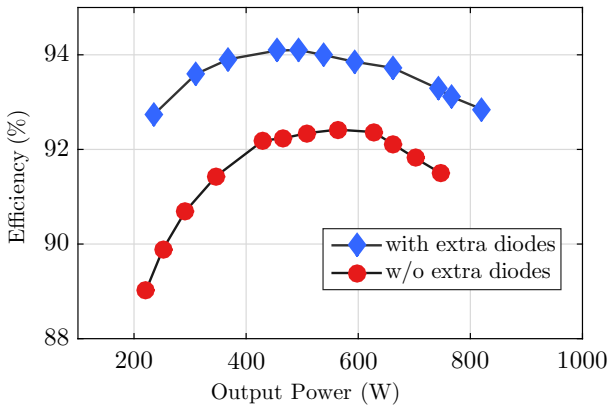

Fig. 21: Efficiency plots for 100 V to 1 kV conversion with and without extra parallel diodes.

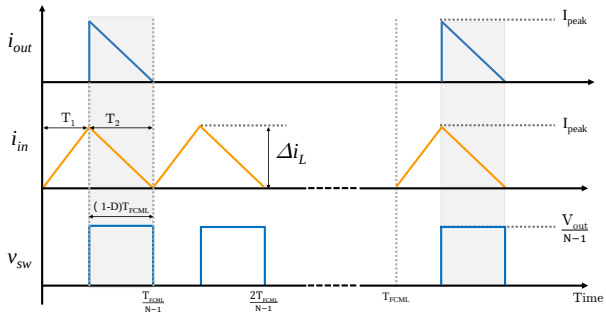

Fig. 22: Output current, inductor current and switching node voltage of FCML in BCM.

and voltage gain. In [44], a conventional boost converter is merged with Cockcroft-Walton Multiplier charge pumps to alleviate the voltage stress on individual switches. It achieved high efficiency and high voltage gain, but the large volume of required capacitors limited the power density. The converter in [45] achieved good voltage gain and efficiency with soft-switching techniques and step-up transformers, but the large size of the magnetic components resulted in low power density. In [33], the inductor size is reduced substantially by switching at very-high frequency and the switching loss is reduced by operating the converter in resonant mode [9]. However, the multiple stage design of matching networks, transformers and rectifiers leads to a relatively low overall system efficiency. Moreover, the passive components in matching networks and the transformer further increase the total volume of the converter. It should be noted that though all these works target at high voltage gain, high efficiency and power density, they have different specifications and application scenarios, which results in different goals for optimization. Therefore, the purpose of Table IV is not to directly compare the specific performance numbers but to demonstrate the potential improvements on power density and efficiency through the FCML approach for high voltage step-up converters.

V. Conclusions

This work presented the design fundamentals and practical implementation considerations of a 7-level FCML boost converter. A prototype converter with compact layout has been implemented and successfully converted 100 V to 1 kV at 820 W output power, with 94.1% peak efficiency reached at 542 W input power, achieving 2342 W/in^3 (143 W/cm^3) power density by passive component volume, 687 W/in^3 (42 W/cm^3) power stage power density and 329 W/in^3 (20 W/cm^3) overall power density. Optimal implementation for flying capacitors at high operating voltage has been discussed. Different diodes have been evaluated for their switching performances. Techniques to reduce reverse recovery loss have been explored and experimented. QSW-ZVS technique can be further investigated using inductors with lower core loss.

VI. Appendix

A. Condition for boundary conduction mode

The detailed derivation for (8) is given in this section. The waveform of output current i_{out} (before the output capacitor), input inductor current i_{in} and switching node voltage v_{sw} in the Boundary Conduction Mode (BCM) operation for the duty ratio condition $D > \frac{N-2}{N-1}$ are illustrated in Fig. 22. The inductor current ramp-up time, label T_1 in Fig.22, is given as

$$T_1 = (\frac{1}{N-1} - (1-D))T_{\text{FCML}}. \tag{11}$$

At BCM, the inductor current swings from zero to twice of the average input current. To ensure the operation in CCM or BCM, the ratio between peak-to-peak ripple current Δi_{L} and the average input current I_{in} cannot be greater than two. This condition is expressed in (12).

$$\frac{\Delta i_{\text{L}}}{I_{\text{in}}} = \frac{V_{\text{in}} T_1}{L_{\text{FCML}} I_{\text{in}}} = \frac{V_{\text{in}}(\frac{1}{N-1} - (1-D))}{L_{\text{FCML}} f_{\text{FCML}} I_{\text{in}}} \leq 2 \tag{12}$$

Since the voltage and current between input and output are related as $V_{\text{out}} = \frac{V_{\text{in}}}{1-D}$ and $I_{\text{out}} = I_{\text{in}}(1-D)$, $\frac{V_{\text{in}}}{I_{\text{in}}}$ can be

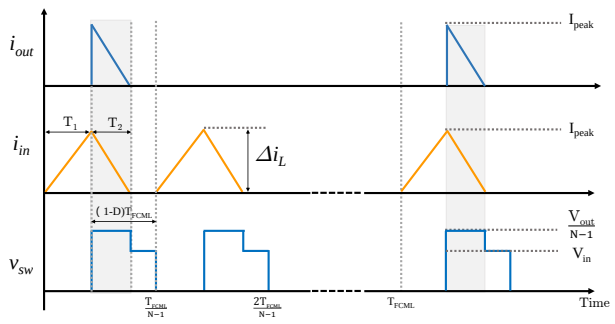

Fig. 23: Output current, inductor current and switching node voltage of FCML in DCM.

expressed with the load resistance R_{out} and the duty ratio D as

$$\frac{V_{\text{in}}}{I_{\text{in}}} = R_{\text{out}}(1-D)^2, \tag{13}$$

substituting (13) into (12), the condition in (8) can be obtained.

B. Conversion ratio in DCM

The inductor current and switching node voltage waveforms in DCM (with ideal switches and ideal diodes) for duty ratio greater than $\frac{N-2}{N-1}$ are shown in Fig. 23. During T_1, the inductor current increases to the peak value as

$$I_{\text{peak}} = \frac{V_{\text{in}}T_1}{L_{\text{FCML}}} = \frac{V_{\text{in}}(\frac{1}{N-1} - (1-D))}{L_{\text{FCML}}f_{\text{FCML}}}. \tag{14}$$

The length of T_2 annotated in Fig. 9 varies with the load current. In one full switching period T_{FCML}, the inductor is directly connected with the output capacitor for T_2 of the time, as shown in Fig. 23. In other words, the frequency of the output current is f_{FCML}, while the frequency of the input current is $(N-1)f_{\text{FCML}}$. Since the average current through the output capacitor is zero, we can express the average output current $I_{\text{out, ave}}$ as

$$I_{\text{out, ave}} = \frac{I_{\text{peak}}T_2}{2T_{\text{FCML}}} = \frac{V_{\text{out}}}{R_{\text{out}}}. \tag{15}$$

Correspondingly, we can also obtain the average input current by calculating the total charge flow over the time period $\frac{T_{\text{FCML}}}{N-1}$ as

$$I_{\text{in, ave}} = \frac{I_{\text{peak}}(T_1+T_2)}{2\frac{T_{\text{FCML}}}{N-1}} = \frac{V_{\text{in}}T_1}{L_{\text{FCML}}}\frac{T_1+T_2}{2\frac{T_{\text{FCML}}}{N-1}}. \tag{16}$$

Assuming constant input and output voltage and negligible losses, the input power equals the output power as

$$V_{\text{in}}I_{\text{in, ave}} = V_{\text{out}}I_{\text{out, ave}}. \tag{17}$$

By substituting in Equation (15) and (16), (17) can be simplified to the quadratic equation

$$V_{\text{out}}{}^2 - V_{\text{in}}V_{\text{out}}(N-1) - \frac{V_{\text{in}}{}^2T_1{}^2R_{\text{out}}(N-1)}{2T_{\text{FCML}}L_{\text{FCML}}} = 0, \tag{18}$$

from which V_{out} can be solved as a variable in terms of V_{in} as shown in (9).

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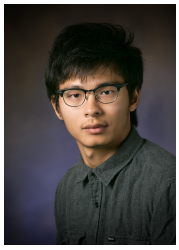

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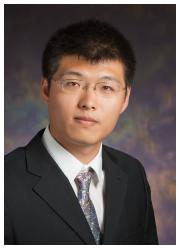

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