A Systematic Design Methodology for Series-Stacked Energy Decoupling Buffers Based on Loss-Volume Pareto Optimization

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***Abstract*—The series-stacked buffer (SSB) is an active twice-line frequency energy decoupling buffer architecture in single-phase converters. The high power density and efficiency characteristics of this architecture have been recently demonstrated. However, in previous hardware work on the SSB, the energy utilization ratios of the buffer capacitors are not optimized, and the tradeoff among loss, volume and bus voltage ripple have not been quantitatively studied. In this work, we propose a methodology that quantifies and formalizes the SSB design process into a multi-objective optimization problem, from which the Loss-Volume Pareto front can be solved, and optimal control strategy for minimum loss can be determined. Design constraints, modeling of objective functions, and optimization algorithms are discussed. With realistic hardware parameters and constraints, this methodology is applied to the SSB design for a 1.5-kW, 400-V dc-bus single-phase system. The corresponding Pareto front results are studied with hardware prototypes. Compared to previous SSB hardware demonstrations, both power density and efficiency of the designed hardwares are substantially enhanced with the proposed method.**

I. Introduction

For single-phase ac-dc and dc-ac converters, an energy decoupling device is required to buffer the instantaneous power mismatch between the ac and dc side at the twice-line frequency. Due to the tight dc-bus voltage ripple requirement, a passive capacitor bank solution at the dc-bus often requires a large capacitance. Such large capacitance is usually implemented with large electrolytic capacitor banks at the dc-bus, which suffer from short lifetime, low temperature range and limited current ripple capability [1]. While film and ceramic capacitors offer better performance for these metrics, their lower energy density becomes the major tradeoff. Thus, to fully utilize the benefit of film or ceramic capacitors for single-phase energy buffering, their energy utilization ratio has to be improved. Active energy buffers, in general, improve the energy utilization ratio of the capacitors by allowing much larger capacitor voltage ripples than the passive capacitor bank solution. However, the extra active power converters and controller often introduce a large penalty in efficiency and circuit complexity in many solutions [2].

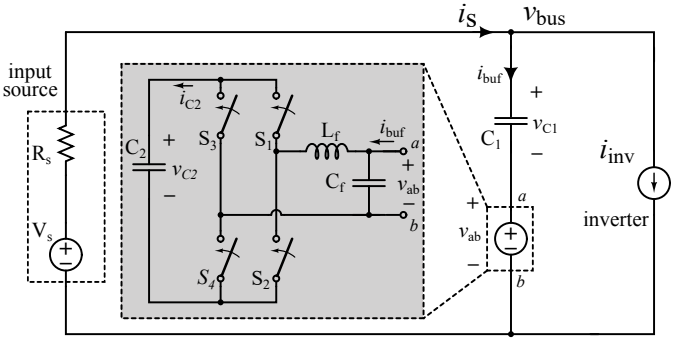

Fig. 1. The series-stacked buffer architecture with a dc source and an inverter (represented as a current load).

The series-stacked buffer (SSB), shown in Fig. 1, is a type of active energy decoupling buffer that is suitable for single-phase converters. The main energy buffering capacitor C_1 stores and releases energy at the twice-line frequency with a large voltage ripple, which allows high energy utilization of the capacitor, compared to the passive capacitor bank solution. A bi-directional full-bridge converter is connected in series with C_1 and generates a terminal voltage v_{ab} that cancels the ripple component on v_{C1} such that the dc-bus is ripple-free. As the high dc-bus voltage is blocked by C_1 from the full-bridge converter, the converter can be implemented with lower voltage rating devices, operating at high switching frequencies to miniaturize the passive components. Moreover, since the bi-directional converter only processes a fraction of the total power in the dc-ac conversion stage, the resulting high overall system efficiency is comparable to the passive capacitor bank solution. The high power density and high efficiency characteristics of the SSB have been demonstrated in [3], [4]. In ideal lossless operation, the SSB has no net energy change in one twice-line frequency cycle. As a result, no active power source is needed and a support capacitor C_2 can instead function as the energy source for the full-bridge. However, in any practical implementation, since the full-bridge converter is lossy, a compensation scheme [4]–[6] is needed to regulate v_{C2} by introducing a small voltage ripple on the dc-bus to draw real power into the buffer converter, preventing v_{C2} from

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decaying. In other words, the magnitude of the dc-bus voltage ripple introduced by the SSB is positively correlated to the power loss in the full-bridge, which is determined by particular hardware design parameters and control strategies in the SSB. For example, one can design the SSB with smaller C_1 and C_2, which leads to larger voltage swing magnitudes during normal operation. Consequently, the voltage stress in the converter is increased, causing higher switching and inductor loss. Thus, inherently, there exists a tradeoff between passive component volumes and losses in the SSB.

However, in previous optimization work [7] on the SSB, the relations among the power loss, bus ripple, and passive component size in the SSB have not been quantified and incorporated into the optimization process. Moreover, the single-constraint, single-objective optimization process based on the Lagrange Multiplier method is unable to solve for the optimal SSB hardware designs with multiple optimization objectives, and under multiple real component constraints. The lack of quantitative analysis on the relations among loss, bus ripple and volume also makes it difficult to comprehensively compare the SSB with other optimized active buffer designs [8]–[10].

Another limitation of previous optimization work is that the energy utilization ratio of C_2 is not optimized due to conservative design constraints [7] [11] and a specific modulation strategy [11]. For a given value of C_1 under a certain load condition, C_2 should satisfy a minimal dc energy storage requirement such that the conversion ratio of the full-bridge is always less than one. Such constraint is derived and verified in [12]. However, in previous hardware demonstrations [4], [11], [13], the stored dc energy on C_2 is much higher than the minimal requirement. Furthermore, since the energy in a capacitor is $\frac{1}{2}CV^2$, there are two specific scenarios of storing excessive energy: either the capacitance of C_2 was oversized for a given dc voltage on C_2, or the dc voltage on C_2 is controlled at a much higher voltage than the lowest voltage defined by the constraint, considering a fixed C_2 capacitance. In the first case, the volume of C_2 is not optimized. In the second case, the loss in the full-bridge is higher than the optimized case due to higher voltage stress. As a result, all previous hardware demonstrations were not on the most optimized Loss-Volume Pareto front.

In this work, we formalize the SSB design process as a multi-objective optimization (MOO) problem under multiple non-linear constraints, which can be solved with numerical analysis tools (Matlab, Python, etc). The over-modulation constraint in [12] is utilized to obtain the designs with optimal energy utilization ratio, which allows the SSB to be compared with other optimized active buffer topologies on common performance metrics. This work is an extension of a previous conference paper [14], with extended analysis on the buffer operation and experimental results, and additional discussion on a generalized design methodology. The structure of this paper is as follows. First, the operation and design constraints of the SSB are presented in Section II. In Section III, the modeling processes for the loss and passive component volume functions are presented. With the constraints and objective functions being identified, Section IV discusses optimization formulation and algorithms. Section V presents the optimization results of the loss-volume Pareto front. Section VI verifies the optimization results with three different hardware designs on the Pareto front. Section VII provides details for practicing engineers on how to generalize the methodology to include more objectives and variables for more comprehensive optimization. Finally, Section VII concludes the paper.

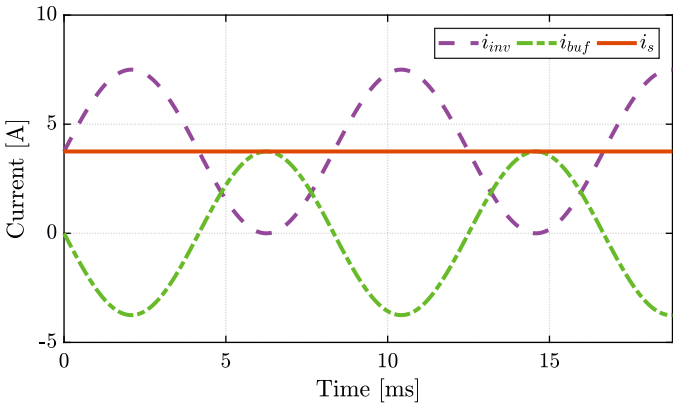

Fig. 2. The ideal current waveforms for the SSB. C_1 = 80 μF, C_2 = 68 μF, V_{bus} = 400 V, 1.5 kW load power.

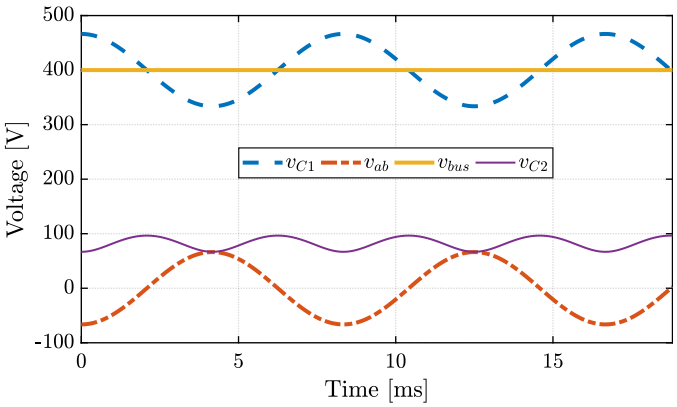

Fig. 3. The ideal voltage waveforms for the SSB. C_1 = 80 μF, C_2 = 68 μF, V_{bus} = 400 V, 1.5 kW load power.

II. Series-Stacked Buffer Operation Constraints

In this section, the operation of the SSB is discussed, and four critical constraints that relate to component design choices are identified, which are noted as g_1, g_2, g_3 and g_4.

In single-phase conversion with unity power factor on the ac-side, the inverter load current (or rectifier input current for the ac-dc case) can be modeled as a dc-shifted sinusoidal current i_{inv} as

$$i_{\text{inv}} = I_{\text{dc}} \sin(\omega t) + I_{\text{dc}} \tag{1}$$

where the constant I_{dc} is the ideal dc-side current, and ω is twice of the line frequency (i.e., $2\pi \times 120$ rad/s, for the U.S. line frequency considered here). Considering the current constraint at the dc-bus (as shown in Fig. 1),

$$i_{\text{S}} = i_{\text{inv}} + i_{\text{buf}} \tag{2}$$

For i_S to be the ideal constant current I_{dc}, the current flowing into the SSB i_{buf} must be purely sinusoidal, canceling the ripple term in (1) as

$$i_{buf} = -I_{dc}\sin(\omega t). \tag{3}$$

The corresponding ideal waveforms of key currents and voltages in the SSB are illustrated in Fig. 2 and Fig. 3. Detailed derivations of expressions for the voltages and currents are given in [4], [5], [12].

A. C_1 Voltage Rating Constraint – g_1

As shown in Fig. 3, the voltage on C_1 ripples around the dc-bus voltage with the sinusoidal current in (3) as

$$v_{C1} = V_{bus} + \frac{I_{dc}}{\omega C_1}\cos(\omega t) \tag{4}$$

whose maximum can be found as

$$v_{C1,\,max} = V_{bus} + \frac{I_{dc}}{\omega C_1}. \tag{5}$$

This maximum voltage has to be lower than the voltage rating on capacitor C_1. This constraint g_1 is expressed as (6) for the optimization problem as

$$g_1 = V_{bus} + \frac{I_{dc}}{\omega C_1} - V_{C1,\,rating} \le 0. \tag{6}$$

B. Full-Bridge Voltage Rating Constraint – g_2

The instantaneous voltage on C_2 can be solved by analyzing the power flow through the full-bridge converter [12] as

$$v_{C2} = \sqrt{V_{C2,\,dc}^2 - \frac{I_{dc}^2}{2\omega^2 C_1 C_2}\cos(2\omega t)} \tag{7}$$

where $V_{C2,\,dc}$ is the dc value of v_{C2}. This operating parameter is maintained with a feedback loop in practical implementations, and will be discussed in later sections. Correspondingly, the maximum value of v_{C2} can be found as

$$v_{C2,\,max} = \sqrt{V_{C2,\,dc}^2 + \frac{I_{dc}^2}{2\omega^2 C_1 C_2}}. \tag{8}$$

Parameter $v_{C2,\,max}$ is the maximum voltage stress in the full-bridge converter, which should not be higher than the minimum of the voltage rating of capacitor C_2 ($V_{C2,\,rating}$) and the switch voltage rating $V_{sw,\,rating}$. This constraint g_2 is expressed as

$$g_2 = \sqrt{V_{C2,\,dc}^2 + \frac{I_{dc}^2}{2\omega^2 C_1 C_2}} - min\{V_{C2,\,rating}, V_{sw,\,rating}\} \le 0 \tag{9}$$

C. Over-Modulation Constraint – g_3

To ensure that the output voltage from the full bridge converter v_{ab} is generated correctly as in (10) to cancel the ripple voltage on v_{C1}, the conversion ratio of the full-bridge converter must not be higher than one.

$$v_{ab} = -\frac{I_{dc}}{\omega C_1}\cos(\omega t). \tag{10}$$

The maximum conversion ratio of the full-bridge converter can be found as

$$\left|\frac{v_{ab}}{v_{C2}}\right|_{max} = \frac{\frac{I_{dc}}{\omega C_1}}{\sqrt{V_{C2,\,dc}^2 - \frac{I_{dc}^2}{2\omega^2 C_1 C_2}}} \le 1 \tag{11}$$

which should not be greater than one. Expression (11) can be simplified to the over-modulation constraint that describes the relation among the capacitance of C_1, C_2, dc voltage level $V_{C2,\,dc}$ of v_{C2}, and ideal dc side current I_{dc} as

$$g_3 = \frac{I_{dc}}{\omega} - C_1 V_{C2,\,dc}\sqrt{\frac{2C_2}{2C_2 + C_1}} \le 0. \tag{12}$$

This constraint is referred to as g_3 in the optimization problem. The detailed derivation and verification with hardware results for this constraint can be found in [12].

D. Inductor Saturation Current Constraint – g_4

The current in the filter inductor L_f in the full-bridge converter should not exceed its saturation current limit. For the full-bridge inverter, the shape of the inductor current is dependent on the types of modulation strategies. The two common fixed-frequency modulation schemes are bipolar and unipolar modulation. Figure. 4 compares the gate signals, inductor voltage and current waveforms of these two modulation schemes with the same duty ratio and average inductor current. If the full-bridge is modulated with bipolar modulation scheme, the inductor peak-to-peak current ripple can be expressed as

$$\Delta I_{L,\,bi} = \frac{(v_{C2} - v_{ab})D}{L_f f_{sw}} \tag{13}$$

where D is the duty ratio of S_1. Since in a full-bridge converter, $v_{ab} = (2D-1)v_{C2}$, (13) can be rewritten in terms of v_{ab} and v_{C2} as

$$\Delta I_{L,\,bi} = \frac{(v_{C2} + v_{ab})(v_{C2} - v_{ab})}{2v_{C2}L_f f_{sw}}. \tag{14}$$

The maximum inductor current ripple occurs when v_{C2} is at its peak, and v_{ab} is at zero volt, which is expressed as

$$\Delta I_{L,\,bi,\,max} = \frac{\sqrt{V_{C2,\,dc}^2 + \frac{I_{dc}^2}{2\omega^2 C_1 C_2}}}{2L_f f_{sw}}. \tag{15}$$

This moment is also when the average inductor current i_{buf} is at its peak of I_{dc}. Consequently, the peak inductor current I_{peak} in one 120 Hz cycle is then

$$I_{peak,\,120Hz} = I_{dc} + \frac{\Delta I_{L,\,bi,\,max}}{2} \tag{16}$$

If the full-bridge is modulated with unipolar scheme, the inductor current ripple is

$$\Delta I_{L,\,uni} = \frac{|v_{ab}|(v_{C2} - |v_{ab}|)}{2v_{C2}L_f f_{sw}}. \tag{17}$$

Notice that the maximum inductor ripple current and the average inductor current within one 120 Hz cycle do not

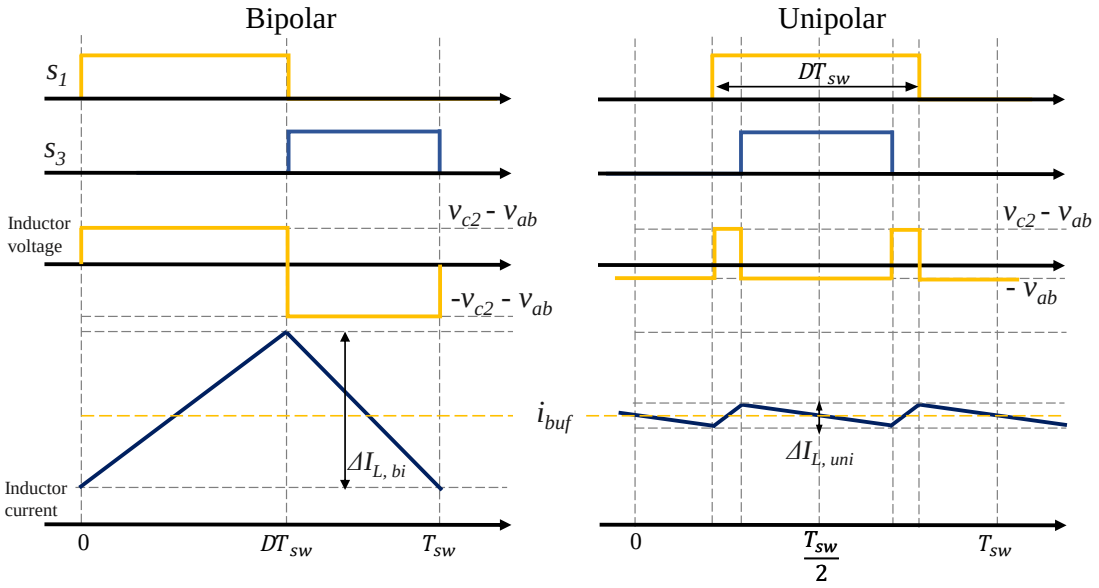

Fig. 4. Gate signals for S_1 and S_3, inductor voltage and current waveforms of bipolar (left) and unipolar modulation (right) in a full-bridge with identical duty ratio and average inductor current.

$$I_{\text{peak, sw}} = \frac{1}{2}\Delta I_{\text{L, uni}} + i_{\text{buf}} = \frac{\left|\frac{I_{\text{dc}}}{\omega C_1}\cos(\omega t)\right|\left(\sqrt{V_{\text{C2, dc}}^2 - \frac{I_{\text{dc}}^2}{2\omega^2 C_1 C_2}\cos(2\omega t)} - \left|\frac{I_{\text{dc}}}{\omega C_1}\cos(\omega t)\right|\right)}{4\sqrt{V_{\text{C2, dc}}^2 - \frac{I_{\text{dc}}^2}{2\omega^2 C_1 C_2}\cos(2\omega t)}L_f f_{\text{sw}}} - I_{\text{dc}}\sin(\omega t) \tag{17}$$

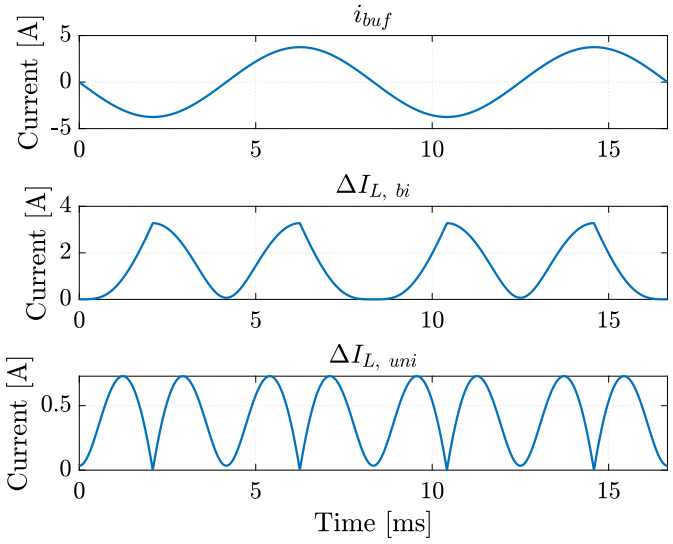

Fig. 5. Waveforms of i_{buf}, $\Delta I_{\text{L, bi}}$, and $\Delta I_{\text{L, uni}}$ under the condition: C_1 = 80 μF, C_2 = 68 μF, V_{bus} = 400 V, L_f= 94 μH, 1.5 kW load power.

happen simultaneously as in the bipolar case. Waveforms for i_{buf}, $\Delta I_{\text{L, bi}}$, and $\Delta I_{\text{L, uni}}$ are plotted for comparison in Fig. 5. Thus, the peak inductor current in one 120 Hz cycle is not as obvious as in the bipolar case. To find the peak inductor current in one 120 Hz cycle, the peak inductor current of each switching cycle is firstly found as (17).

The maximum of (17) is the maximum inductor current within one 120 Hz cycle, $I_{\text{peak, 120Hz}}$. However, the explicit solution of the maximum is complicated to derive. To solve the maximum of (17) numerically, (17) is discretized into an array within one 120 Hz cycle, and the maximum value in the array can be found using numerical analysis tools.

In both cases of modulation, the peak inductor current within one 120 Hz cycle $I_{\text{peak, 120Hz}}$ has to be lower than the saturation current limit $I_{\text{sat, limit}}$ of the inductor. This constraint g_4 is expressed as

$$g_4 = I_{\text{peak, 120Hz}} - I_{\text{sat, limit}} \leq 0. \tag{19}$$

To minimize filter capacitor size and inductor ripple current, unipolar modulation is studied in the optimization and applied to the hardware design.

III. Loss and Volume Objective Functions

To study the trade-off between loss and volume of the SSB, a loss function f_{loss} and a volume function f_{volume} are developed.

A. Loss function – f_{loss}

The loss function of the SSB is developed based on the loss model for full-bridge buck converters. Conduction loss P_{cond}, switching loss P_{sw} and inductor loss P_{L} are included. EPC2033 GaN switch is used in the loss modeling as well as the final hardware implementation. As both C_1 and C_2 are constructed with many individual capacitors in parallel, with correspondingly low equivalent series resistance (ESR), the loss from the capacitors are omitted. It should be noted that accurate loss modeling itself is a subject of research [15]. The objective here is to obtain high level loss models to be

used in the optimization. More detailed loss models can be incorporated into the optimization technique as they become available and are validated against hardware.

1) Conduction loss P_{cond}: During the process to compute the optimization results, it is not guaranteed that the inductor current ripple is negligible in all designs. Thus, the inductor current ripple has to be considered to calculate the RMS current. Considering unipolar modulation, the amplitude of the current ripple varies with the voltage across the inductor within one 120 Hz cycle as expressed in (17). The RMS current of each switching cycle is computed, summed and averaged over one 120 Hz cycle. And since two transistors are conducting in both switching states in one switching cycle in the full bridge converter, the 120 Hz cycle average conduction loss can be calculated as,

$$P_{\text{cond}} = 2R_{\text{ds, on}}\left(\frac{I_{\text{dc}}^2}{2} + \sum_{n=1}^{f_{\text{sw}}/f_{\text{2L}}} \frac{\Delta I_{\text{L, uni}}(t)^2}{12}\frac{f_{\text{2L}}}{f_{\text{sw}}}\right), t = \frac{n}{f_{\text{sw}}} \quad (20)$$

where $R_{\text{ds,on}}$ is the on-resistance of the transistor, and $f_{\text{2L}} = 120$ Hz. In this work, the EPC2033 GaN device was used in the design, and the dynamic $R_{\text{ds,on}}$ effect [16] has been taken into consideration in the loss model.

2) Switching loss P_{sw}: In the full-bridge converter, all switches need to block v_{C2} and carry the average inductor current i_{buf}. The overlap switching loss and C_{oss} loss of the GaN transistors are included in the loss model.

Since both v_{C2} and i_{buf} are periodic signals with 120 Hz frequency, in order to calculate the 120 Hz cycle average switching loss P_{sw}, first of all, the energy losses of all switching instants within one 120 Hz cycle are summed up as

$$E_{\text{overlap}} = \sum_{n=1}^{f_{\text{sw}}/f_{\text{2L}}} (v_{\text{c2}}(t)|i_{\text{buf}}(t)|)(t_{\text{on}} + t_{\text{off}}),\ t = \frac{n}{f_{\text{sw}}} \quad (21)$$

where t_{on} and t_{off} are the transition times of each turn-on and turn-off switching actions, calculated from the gate charge in the device datasheet and the chosen gate resistance.

As the energy dissipation in the output capacitance C_{oss} of the GaN transistors also changes with v_{C2} for each switching cycle, the total energy loss in C_{oss} in one 120 Hz cycle E_{coss} is obtained in a similar way as the overlap energy loss. Consequently, the average switching power loss in one 120 Hz cycle can be obtained as

$$P_{\text{sw}} = (E_{\text{overlap}} + E_{\text{coss}})f_{\text{2L}}. \quad (22)$$

3) Inductor loss P_L: Similarly, as v_{C2}, v_{ab} and i_{buf} change for each switching cycle within one 120 Hz cycle, the core loss, ac loss and dc resistance loss in the inductor also need to be calculated as the 120 Hz cycle average. In this work, the loss model from Vishay [17] is used to obtain the loss from the voltage and current waveforms on the inductor. The model which includes core loss, ac loss, and DCR loss is expressed as

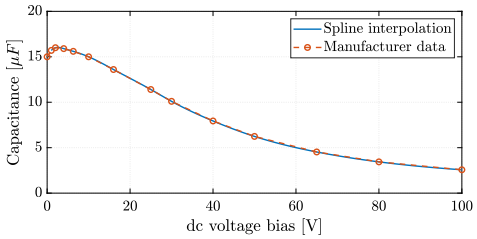

Fig. 6. Manufacturer's data and spline interpolation for dc voltage bias v.s. Capacitance characteristic for TDK CGA9.

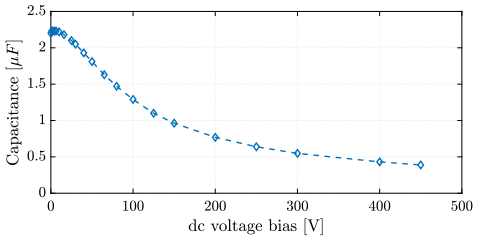

Fig. 7. Manufacturer's data for dc voltage bias v.s. Capacitance characteristic for TDK C5750

$$\begin{aligned} P_L &= P_{\text{core}} + P_{\text{ac}} + P_{\text{DCR}} \\ &= k_0 f_e^{k_f - 1} B_{pk}{}^{k_b} f_0 \times 10^{-14} + k_1 \Delta I^2 \sqrt{f_0} R_{\text{OPER}} + I_{\text{dc}}^2 R_{\text{OPER}}, \end{aligned} \quad (23)$$

where k_0, k_1, k_b, k_f and R_{OPER} are inductor parameters from the datasheet, f_0 is the switching frequency, B_{pk} is the peak magnetic field, ΔI is the peak-to-peak current ripple, and I_{dc} is the average dc current.

B. Volume function – f_{volume}

Since capacitor C_1 and C_2 dominate the total volume of the SSB, the volume function is modeled as the total volume of capacitors used for C_1 and C_2. To achieve state-of-the-art power density, X6S and X7S multi-layer ceramic capacitors (MLCC) with high energy density listed in Table I are chosen for hardware implementation. A suitable number of capacitors are connected in parallel to achieve the desired capacitance values for C_1 and C_2. As the capacitance of X6S and X7S ceramic capacitors decreases as the dc voltage bias increases, the characteristic data from the manufacturer are used to calculate C_2's capacitance as a function of dc voltage bias $V_{\text{C2, dc}}$. As 14 data points on the characteristic curves are provided by the manufacturer, spline interpolation is used to obtain values between the given data points, as shown in Fig. 6. For C_1, the capacitance at 400 V is used in the calculation. As discussed in [18], the change in capacitance with dc-bias voltage will distort current through the ceramic capacitors if a large voltage swing is applied. However, in the SSB operation, since both v_{C1} and v_{C2} already have relatively high dc-bias levels compared to their ripple components, the corresponding ranges of voltage swing will not cause too much change in the capacitance. Moreover, as the voltage swings below and above the dc-bias point in one 120 Hz cycle, the average effective capacitance is very close to the value at the dc-bias voltage.

Finally, as the manufacturer's characteristic curve of C_1 (TDK C5750) in Fig. 7 suggests, above 350 V, the rate of change in capacitance vs. voltage is lower than that at lower voltages. For the above reasons, the non-linearity and distortion effect identified in [18] can be omitted in this work for optimization purposes.

Correspondingly, the number of ceramic capacitors needed and their total volume can be obtained by (24), where $\text{Vol}_{\text{C5750}}$ and Vol_{CGA9} are the volumes of individual capacitors as in Table I.

$$\begin{aligned} f_{\text{volume}} = & \frac{C_1}{C_{\text{C5750, derated}}(V_{\text{bus}})}\text{Vol}_{\text{C5750}} \\ & + \frac{C_2}{C_{\text{CGA9, derated}}(V_{\text{C2,dc}})}\text{Vol}_{\text{CGA9}}. \end{aligned} \tag{24}$$

IV. Optimization Formulation

As power converter design is a multi-dimensional problem in both variable and objective space, there are certain tradeoffs between high order of dimensions and low order of dimensions for the optimization. For optimization that includes many variables and objectives, while the results are more comprehensive, they often do not provide an intuitive understanding of how a particular variable affects the optimization results, and what are the tradeoffs among certain design variables. For optimization that are constrained to fewer variables, though the results are not as comprehensive and might not capture the most optimized design, the effects of certain variables can be isolated and studied, and tradeoffs can be intuitively understood. The loss-volume, or Efficiency-Power Density Pareto front study is one of the common multi-objective studies to determine tradeoffs and the achievable design space of a power converter [8], [19].

For this work, the goal is to quantitatively understand a few particular tradeoffs within the SSB design parameters and verify the models and optimization results with hardware, yet we would also like the results to simultaneously be close to the most optimized design. As such, the inductor is chosen to be fixed for the optimization procedure for mainly two reasons: 1) As briefly mentioned in the introduction, the SSB topology allows the use of lower voltage rating devices in the full bridge, operating at high switching frequencies. Moreover, the power processed by the full-bridge converter in the SSB is lower than a full ripple port buffer [8]. As such, the volume of L_f is relatively small compared to the total volume of C_1 and C_2. 2) Since C_1 and C_2 are constructed with many small MLCC capacitors, the relation between the total volume and capacitance can be well defined as a continuous function in (24). However, since the volume of an inductor depends on many practical considerations during construction, the relation between the physical volume of the inductor and the inductance are more complicated to model as a single closed-form function. While a simplified first-order model for the inductor volume can be used to study a general trend, the results are unlikely to be directly implemented in actual hardware designs.

Another parameter that is fixed in this optimization is the switching frequency of the full-bridge. As briefly discussed in the introduction, changing the relative size of C_1 and C_2 would change the voltage stress in the full-bridge. Moreover, for the same set of C_1 and C_2, controlling $V_{\text{C2, dc}}$ to be at different levels also affects the voltage stress in the converter. To study the variables relevant to the voltage stress, the influence of the switching frequency on the losses has to be isolated from the study. Thus, three parameters: f_{sw}, L_f and C_f are fixed for a relatively conservative current ripple, and their values are presented in Table II with other component rating limits. The specifications for the inductor used in this design are also listed in Table III. However, it should be noted that both inductor sizing and frequency variations can be incorporated into the general optimization techniques and circuit operating constraints developed in this work, if so desired.

Consequently, both design constraints and objectives are the functions of three variables: C_1, C_2, and $V_{\text{C2, dc}}$. Thus, the design variable vector, $\mathbf{x}$, for the optimization is comprised as

$$\mathbf{x} = [C_1, C_2, V_{\text{C2, dc}}]. \tag{25}$$

To identify the optimal design candidates on the Pareto front, the Weighted Sums method [20] is used. To improve the convergence of the weighted sums method, the design vector $\mathbf{x}$ and objectives (loss and volume) are normalized. The design variables are linearly scaled from zero to one. The physical limits of the design variables are presented in Table IV. Both objectives are normalized about their optimized objective values to bring the order of both objectives near one. This is a common technique to improve the numerical stability of the optimization procedure. The loss objective function is normalized by the highest loss result $F_{\text{loss, max}}$. To obtain this value, the following single-objective non-linear programming optimization problem is solved with Matlab `fmincon()` function to find the design with the smallest volume and highest loss as

$$\begin{aligned} \min_{\mathbf{x}} \quad & f_{\text{volume}}(\mathbf{x}) \\ s.t. \quad & g_i(\mathbf{x}) \leq 0 \quad \forall i = 1, .., 4. \end{aligned} \tag{26}$$

Similarly, the volume objective function is normalized by the largest volume result $F_{\text{volume, max}}$, which is obtained by solving for the design with lowest loss and largest volume as

$$\begin{aligned} \min_{\mathbf{x}} \quad & f_{\text{loss}}(\mathbf{x}) \\ s.t. \quad & g_i(\mathbf{x}) \leq 0 \quad \forall i = 1, .., 4. \end{aligned} \tag{27}$$

The normalized loss-volume optimization problem can be then formalized as

$$\begin{aligned} \min_{\mathbf{x}} \quad & \alpha \cdot \frac{f_{\text{loss}}(\mathbf{x})}{F_{\text{loss, max}}} + (1-\alpha) \cdot \frac{f_{\text{volume}}(\mathbf{x})}{F_{\text{volume, max}}} \\ s.t. \quad & g_i(\mathbf{x}) \leq 0 \quad \forall i = 1, .., 4. \end{aligned} \tag{28}$$

where α is the weighting parameter in the Weighted Sums method. The Pareto front is generated by incrementally varying the weighting parameter α, from 0 to 1 between each optimization procedure. The previously solved two design cases with $F_{\text{volume, max}}$ and $F_{\text{loss, max}}$ are located at the two

TABLE I
CERAMIC CAPACITORS FOR IMPLEMENTING C_1 AND C_2

	Part No.	Voltage rating	Capacitance (@ 0 V dc bias)	Volume
Capacitor for C_1	TDK C5750X6S2W225K250KA (X6S)	466 V	2.2 μF	79.8 mm^3
Capacitor for C_2	TDK CGA9P3X7S2A156M250KB (X7S)	100 V	15 μF	71.3 mm^3

TABLE II
CONSTANTS IN THE OPTIMIZATION

f_{sw}	L_f	C_f	$I_{sat,\ limit}$	$V_{C2,\ rating}$	$V_{C1,\ rating}$
150 kHz	94 μH	4 μF	8.6 A	100 V	466 V

TABLE III
SPECIFICATIONS OF THE INDUCTOR USED IN THE DESIGN

Part No.	Vishay IHLP6767GZER470M11 $\times$ 2
Inductance	47 μH $\times$ 2
DCR	40.7 mΩ $\times$ 2
Saturation current	8.6 A
Dimensions	(17.15 mm $\times$ 17.15 mm $\times$ 7 mm) $\times$ 2

ends on the Pareto front. Intermediate values of α will result in designs that lie on a curve between these two anchor points, as shown in Fig. 8. The number of increments in α is the number of design points on the final Pareto front. For each value of α, the optimization problem in (28) is solved to convergence using the interior point algorithm in Matlab `fmincon()` function. To summarize and visualize the proposed methodology for modeling and optimization, a flow chart is developed as shown in Fig. 9. As illustrated in Fig. 9, there are three inputs to formulate a MMO problem: objective functions, design constraints and design variables. The component characteristics and control strategies are linked to the optimization formulation with the loss, volume functions of individual components, voltage and/or current ratings, and design variables to optimize.

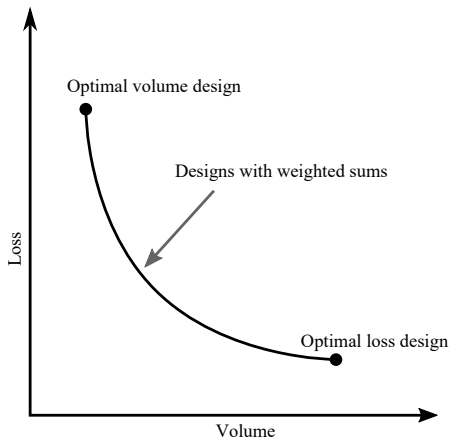

Fig. 8. Pareto front example. The curve illustrates the trade-off between the loss and the volume within achievable design space.

TABLE IV
UPPER LIMITS OF DESIGN VECTORS IN THE OPTIMIZATION

Design variables	C_1	C_2	$V_{C2,dc}$
Limits	500 μF	900 μF	100 V

V. OPTIMIZATION RESULTS

By sweeping α from 0 to 1 with $\frac{1}{30}$ increment, a Loss-Volume Pareto front for 1.5 kW, 400 V dc-bus SSB designs are generated with Matlab in Fig. 10. The purposes of this section are to interpret the Pareto front results to help understand the design process, discuss design trade-offs and establish comparison metrics with other buffer solutions.

A. Volume composition

The compositions of the total volume for all design choices on the Pareto front are plotted in Fig. 11. As can be seen, the volume of C_1 dominates the total volume for all designs due to lower capacitance density at 400 V. With α starting at zero, C_1 is minimized to the capacitance with the highest voltage ripple allowed by constraint g_1, and C_2 is minimized to the capacitance that corresponds to the highest voltage ripple allowed by either constraint g_2 or g_4. For the specific inductor and switching frequency considered here, the peak voltage on C_2 is constrained by g_2 with the capacitor voltage rating. As α starts to increase from zero, C_1 remains at the minimum capacitance, and C_2 is increased to lower the peak voltage stress in the full-bridge. As α further increases, it becomes more important to lower the loss in the objective function, with subsequent increases of C_1 with α. With α = 1, the design is bounded by the upper limits in Table IV.

Compared to the previous SSB design in [4], the percentage of C_2's volume in the total volume is much reduced. Fundamentally, the proposed optimization scheme is able to identify the minimal required energy storage on C_2 under the four design constraints to improve the energy utilization ratio, whereas the design in [4] oversized C_2 with conservative design constraints [12]. A detailed comparison to previous work with hardware results is performed in Section V.

B. Loss composition

The compositions of the losses for all design choices on the Pareto front are plotted in Fig. 12. As can be observed, for the single-phase conversion scenario considered and the choices of components in this study, the switching loss and inductor loss are the two major loss mechanisms compared to the conduction loss. Both switching loss and inductor loss are heavily related to the voltage stress in the full-bridge converter,

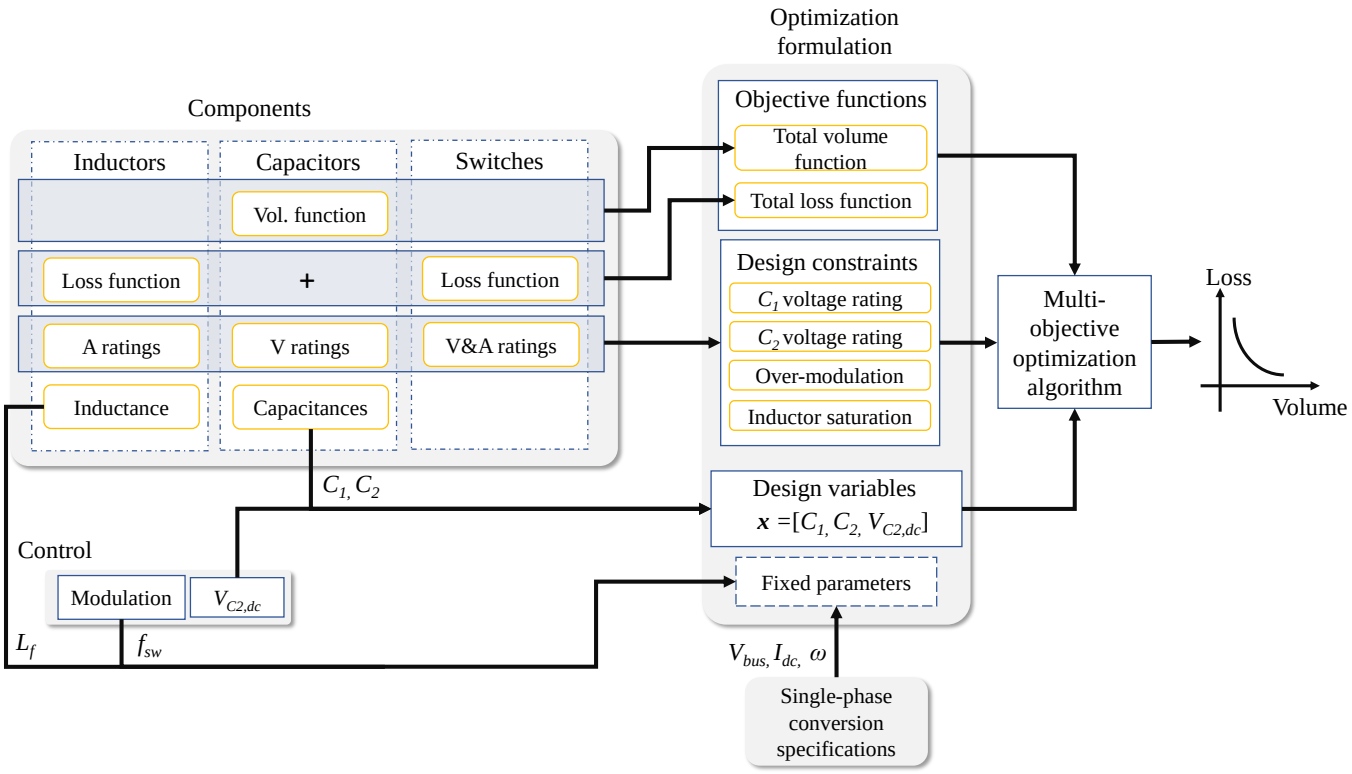

Fig. 9. Design flow chart for the proposed optimization methodology.

which is decided by $V_{\text{C2, dc}}$. The corresponding $V_{\text{C2, dc}}$ for each design is plotted with the loss composition. As discussed in the volume composition subsection, the design with the highest loss and lowest volume is bounded by the design constraint g_1 or g_2. Yet, the design with the lowest loss is bounded by the upper limits of design variables in Table. IV.

Note that the optimized $V_{\text{C2, dc}}$ values in Fig. 12 are for the operation at 1.5 kW. To minimize the loss for any load for a given design of C_1 and C_2, $V_{\text{C2, dc}}$ should be scaled with the load current, or the magnitude of the voltage ripple on C_1: $\Delta v_{\text{C1, max}}$, as shown in the control scheme in Fig. 13. The scalar k between $\Delta v_{\text{C1, max}}$ and $V_{\text{C2, dc}}$ can be determined with the over-modulation design constraint g_3. By rewriting g_3, the constraint for the scalar k is given as

$$k = \frac{V_{\text{C2, dc}}}{\Delta v_{\text{C1, max}}} \geq \sqrt{\frac{2C_2 + C_1}{2C_2}}. \tag{29}$$

As can be seen, the constraint for k is only related to the relation between the capacitance of C_1 and C_2. And to minimize the loss in the converter, k should be set to be as close as possible to the lower bound for lowest voltage stress. Though in previous work [4], $V_{\text{C2, dc}}$ was also scaled with the load current, the scaler was empirically determined, which was higher than the quantitative limit in (29). As a result, the loss was not optimized in the hardware prototype across the full load range.

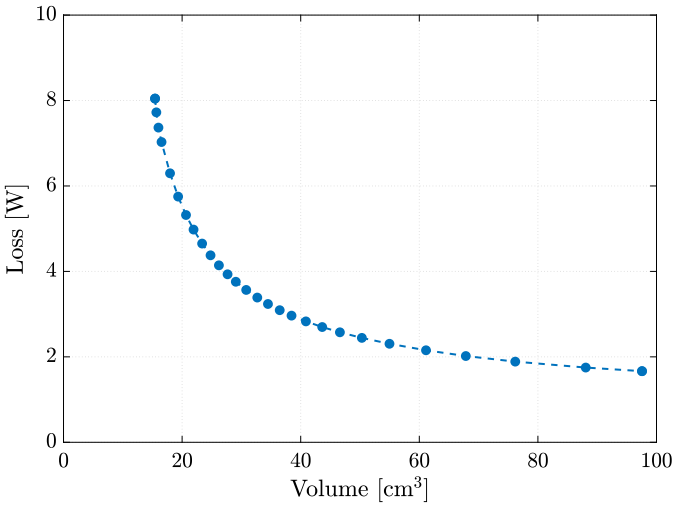

Fig. 10. Generated Loss-Volume Pareto front curve.

C. Dc-bus voltage ripple analysis

Since the full-bridge converter is lossy, a compensation scheme [4], [5] is needed to regulate v_{C2} by introducing a small voltage ripple $v_{\text{ab, com}}$ across terminal ab. This voltage ripple is in-phase with the buffer current i_{buf} to draw real power into the buffer converter, preventing v_{C2} from decaying. This scheme is noted as *Loss compensation for* C_2 in Fig. 13. Since ideally the voltage ripple on C_1 is canceled perfectly, the voltage ripple on the dc-bus is exactly $v_{\text{ab, com}}$. The loss in the SSB P_{loss} and the extra dc-bus peak-to-peak ripple $\Delta v_{\text{bus, pk-pk}}$

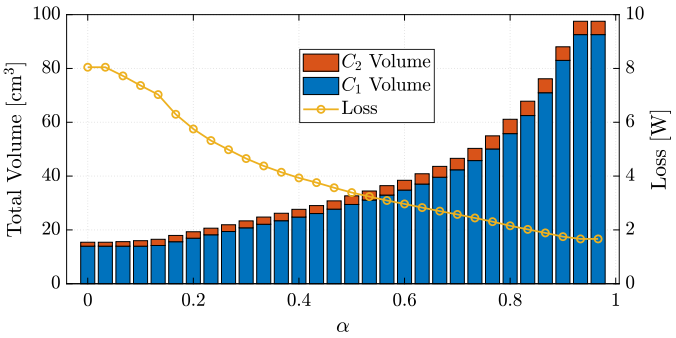

Fig. 11. Generated optimized volume of C_1 and C_2 for all design choices on the Pareto front, plotted with corresponding total loss for each α increments.

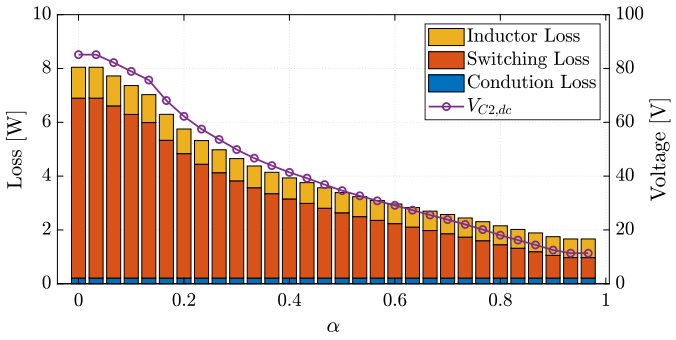

Fig. 12. Generated loss breakdown for all design choices on the Pareto front, plotted with corresponding $V_{C2,\,dc}$ for each α increments.

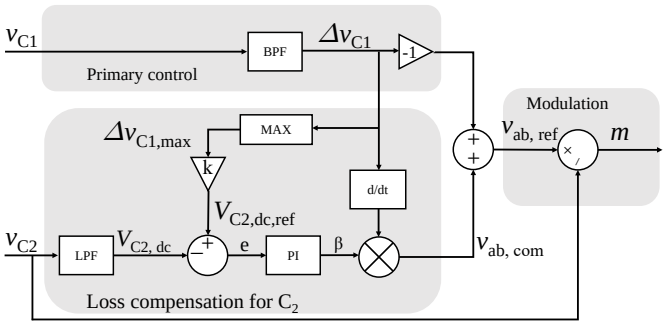

Fig. 13. Control scheme for the SSB. The loss compensation for C_2 introduces extra ripple on the dc bus.

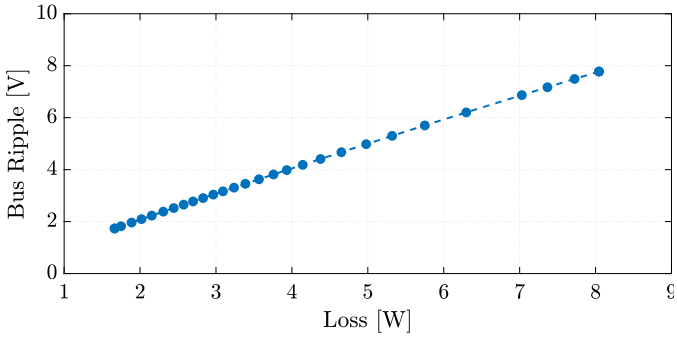

Fig. 14. Calculated compensation ripple $\Delta v_{\text{bus, pk-pk}}$ vs. loss in the SSB P_{loss}, for all design choices on the Pareto-front. Source resistance R_s = 10 Ω.

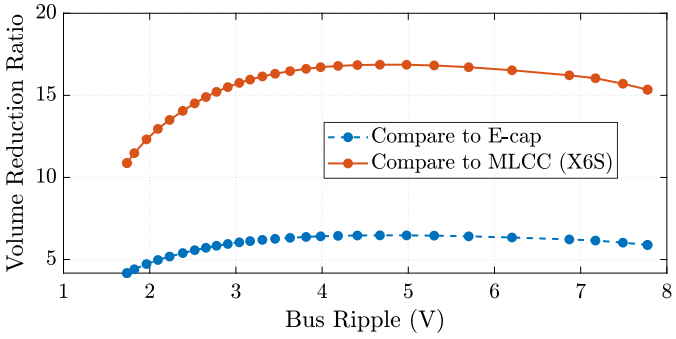

Fig. 15. Volume reduction ratio of the SSB compared to passive capacitor bank solutions vs. bus ripple.

for loss compensation holds the relation as

$$\Delta v_{\text{bus, pk-pk}} = -I_{\text{dc}}R_{\text{S}} + \sqrt{(I_{\text{dc}}R_{\text{S}})^2 + 8P_{\text{loss}}R_{\text{S}}}. \tag{30}$$

Detailed derivation of (30) is given in the appendix.

With an example source resistance $R_{\text{S}} = 10\ \Omega$, the corresponding $\Delta v_{\text{bus, pk-pk}}$ for each design choice on the Pareto front in Fig. 10 can be calculated based on their losses, and plotted in Fig. 14.

In practical applications, the input current ripple or the dc-bus voltage ripple have to remain below certain limits. For example, the Google Little Box challenge requires the input current ripple ratio to be lower than 20% [21], which corresponds to 1 A ripple current limit. Thus, an upper bound of the loss in the SSB can be calculated from (30). Graphically, it is a horizontal line that represents a loss value in Fig. 10, and any design points on the Pareto front that are located above this line should not be considered for implementation. Alternatively, the current ripple limit can also be incorporated into the MOO problem as one of the design constraints such that the all calculated optimization results satisfy the ripple requirement.

D. Equivalent capacitance analysis

To compare the size of the SSB to the conventional electrolytic capacitor bank solution, the equivalent capacitance for an ideal electrolytic capacitor bank (i.e., without ESR) can be computed from $\Delta v_{\text{bus, pk-pk}}$. As the electrolytic capacitor bank buffers the pulsating power at twice the line frequency, the relation between the bus ripple $\Delta v_{\text{bus, pk-pk}}$ and the required capacitance is given as

$$C_{\text{buf}} = \frac{I_{\text{dc}}}{\omega_{\text{line}}\Delta v_{\text{bus, pk-pk}}}. \tag{31}$$

We benchmark the capacitance density (capacitance per volume) of Nichicon UCP2W121MHD6 to calculate the corresponding physical volume of the required electrolytic capacitor as

$$\text{Vol}_{\text{E-cap}} = \frac{C_{\text{buf}}}{\rho_{\text{E-cap}}} \tag{32}$$

where $\rho_{\text{E-cap}}$ = 14 μF/cm^3 for Nichicon UCP2W121MHD6.

If multi-layer ceramic capacitors (MLCC) are used to construct the passive buffer, the capacitance density of TDK

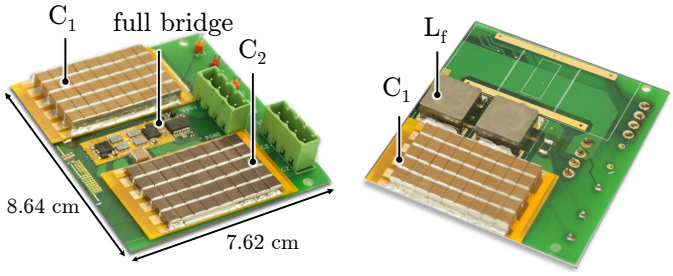

Fig. 16. Photos (top and bottom) of the 1.5 kW SSB hardware test bed. The capacitors are soldered on the yellow daughter boards for the ease of adjustment during testing.

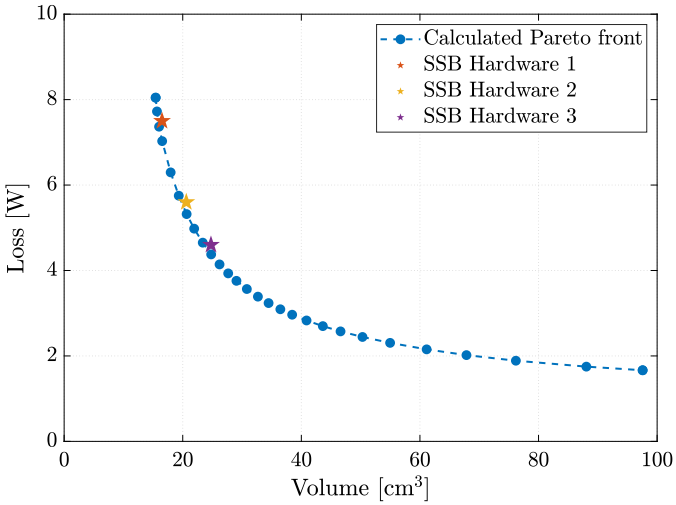

Fig. 17. Measured loss and component volume of three hardware configurations, plotted with the calculated Loss-Volume Pareto-front curve

C5750X6S at 400 V (ρ_{MLCC} = 5.4 μF/cm^3) is used to calculate the physical volume of the total capacitors needed Vol_{MLCC}.

Once the required $\text{Vol}_{\text{E-cap}}$ and Vol_{MLCC} are obtained from corresponding bus voltage ripples, the volume reduction ratio of each SSB design on the Pareto-front compared to passive capacitor bank solutions can be plotted in Fig. 15. As can be observed, within the plotted bus ripple range, the SSB can achieve more than five times reduction on capacitor volume compare to conventional electrolytic capacitor bank solutions.

VI. Hardware Verification

In order to verify the calculated Loss-Volume trade-off, a SSB hardware test bed has been developed as shown in Fig. 16. The ceramic capacitors are soldered on separate daughter boards to test combinations of C_1 and C_2 at different locations on the Pareto front. Three hardware prototype with different parameters as listed in Table V are built and experimentally verified, with all efficiency measurements obtained using Yokogawa WT3000 power meters with high precision. The volume and measured power loss at 1.5 kW of each hardware prototype is plotted along with the calculated Pareto front in Fig. 17. As can be seen, the measured losses are very close to the calculated values for each design, and demonstrate similar loss-volume trade-off trends as the generated Pareto-front design sets, which verifies the practicability of the developed loss and volume models, as well as the optimization process.

The operation waveforms of the three tested hardware prototypes at 1.5 kW are given in Fig. 18, Fig. 19, and Fig. 20, for hardware 1, 2, and 3 respectively. The dc-bus voltage is ac-coupled on the oscilloscope to measure the peak-to-peak ripple voltage. As expected, hardware 1 introduced the largest peak-to-peak bus ripple of 8.5 V, with the highest loss. Hardware 2 and 3 introduced bus ripple voltage of 6 V and 4.8 V respectively.Note that the low frequency noise in Fig. 18, Fig. 19, and Fig. 20 were caused by wire parasitic inductance during the zero-crossing of v_{ab}. Extra wires were used to connect different capacitor boards to vary the capacitor counts for 3 hardware prototypes. From (30), a corresponding bus ripple voltage can be calculated from the measured loss. However, the calculated ripple from the measured loss and the actual measured bus ripple might have some discrepancies as shown in Table VI. This slight deviation can be caused by errors in the ADC and sensing circuits in the controller and/or measurement errors in the power meter. Moreover, the source resistance R_s can also vary with temperatures during testing.

The efficiency of the SSB can be defined in several ways [4], [11]. As the SSB is usually connected at the dc-bus, it is cascaded between the dc source and the inverter (or PFC and the load for ac-dc), the 2-port efficiency is more convenient in terms of calculating efficiencies within a system with multiple stages of converters. In the dc-ac case, the 2-port efficiency is defined as

$$\eta = 1 - \frac{P_{\text{loss}}}{P_{\text{dc}}} \tag{33}$$

where P_{dc} is the average dc power ($V_{\text{bus}} I_{\text{dc}}$).

The 2-port efficiencies at 1.5 kW for three hardware prototypes are also listed in Table V. For hardware 1 and 3, the 2-port efficiencies across the full load range are also plotted for comparison in Fig. 21. Thanks to the control scheme in Fig. 13 to control $V_{\text{C2, dc}}$ to the lowest possible level for every load point, the efficiencies remain very high even at light load conditions for both hardware designs.

To demonstrate that the proposed method has optimized the energy utilization of the capacitors, Table VII lists previous hardware demonstrations for comparison. For hardware in [4], as the exact same types of capacitors for C_1 and C_2 are used in the design, the volume composition can be directly compared. Comparing hardware 1 in this work with the SSB in [4], the percentage of C_2's volume in the total capacitor volume decreases from 32% to only 13%, resulting in 17% increase in power density and slight improvement in efficiency due to more optimized $V_{\text{C2,dc}}$ control. While [11], [13], [22] use different types of capacitors in the design such that the volume cannot be fairly compared, it can be readily observed that the capacitance of C_2 is much larger than C_1 in both hardware demonstrations, which is the result of using conservative operating constraint. A quantitative metric to fairly compare the energy utilization of C_2 is the maximum conversion ratio of the full-bridge in (11), which should be close to one to fully utilize C_2's energy. The maximum conversion ratio can be calculated from C_1, C_2 and $V_{\text{C2, dc}}$ values provided in the literatures using (11), which is 0.85 for [4], 0.68 for [11],

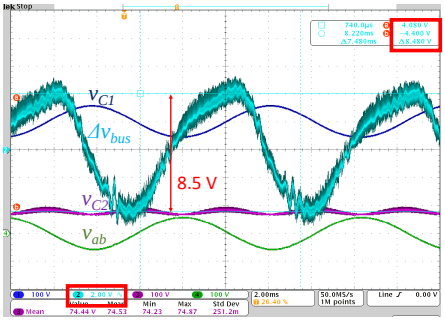

Fig. 18. 1.5 kW, 400 V dc-bus operation waveform of the SSB hardware prototype 1. Bus voltage is ac-coupled to show the ripple component.

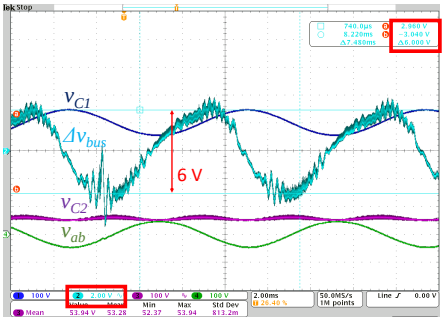

Fig. 19. 1.5 kW, 400 V dc-bus operation waveform of the SSB hardware prototype 2. Bus voltage is ac-coupled to show the ripple component.

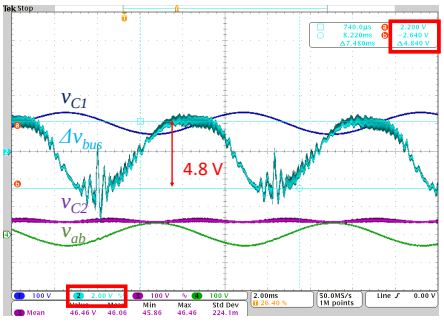

Fig. 20. 1.5 kW, 400 V dc-bus operation waveform of the SSB hardware prototype 3. Bus voltage is ac-coupled to show the ripple component.

TABLE V
DESIGN PARAMETERS FOR THREE TESTED HARDWARES IN THIS WORK

	Hardware 1	Hardware 2	Hardware 3
No. of capacitors for C_1 (volume)	180 (14.36 cm^3)	225 (17.96 cm^3)	270 (21.55 cm^3)
Equivalent large-signal capacitance for C_1 @ 400 V	77.4 μF	96.8 μF	116.1 μF
No. of capacitors for C_2 (volume)	30 (2.14 cm^3)	37 (2.64 cm^3)	45 (3.21 cm^3)
Equivalent large-signal capacitance for C_2 @ $V_{C2,\,dc}$	107.2 μF	217.3 μF	315.4 μF
$V_{C2,\,dc}$ at 1.5 kW	74 V	54 V	46 V
Power density by component volume (C_1,C_2,L_f)	72.8 W/cm^3	60.7 W/cm^3	52.0 W/cm^3
2-port efficiency @ 1.5 kW	99.50%	99.63%	99.69%

TABLE VI
CALCULATED AND MEASURED RIPPLE COMPARISON

Hardware No.	1	2	3
Measured loss at 1.5 kW (W)	7.5	5.6	4.6
Calculated bus ripple from loss (V)	7.2	5.5	4.6
Measured bus ripple (V)	8.5	6.0	4.8
Dc bus voltage ripple ratio	2.1%	1.5%	1.2%
Dc current ripple ratio	22%	16%	13%

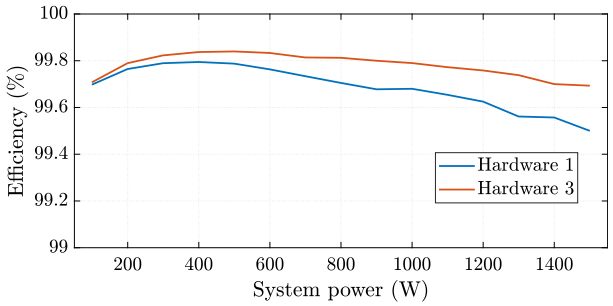

Fig. 21. Efficiencies of hardware 1 and 3 across the full load range.

[13], and 0.82 for [22]. Whereas for both the computed Pareto designs and the tested hardware prototype 1, 2 and 3 in this work, the maximum conversion ratios are all approximately one.

VII. GENERALIZED DESIGN PROCESS

So far, the optimization is constrained for a given inductor with fixed-frequency modulation. In this way, the loss and volume tradeoff caused by the relation among C_1, C_2 and $V_{C2,\,dc}$ can be studied in detail and independently from other variables. Moreover, the optimization results are directly applied to real hardware designs and verified with experiments. However, the framework of the proposed optimization methodology can also be generalized for more comprehensive optimizations, as shown in Fig. 22. Compared to the design process in Fig. 9, both f_{sw} and L_f are set as design variables instead of fixed parameters. The volumes, losses and V&A ratings of capacitors, inductors and switches are all considered in the model.

It should be noted that volume functions for both capacitors and inductors are preferred to be continuous in this generalized design process to improve the numerical stability for the optimization procedure. For instance, a general capacitance/inductance (per volume) density can be used to estimate the needed volumes [23]. Yet, the results might not be as practical, unless the degree of freedom in the actual capacitor and inductor design and manufacturing is high [24]–[26].

If a large component database is linked to the procedure, to optimize the buffer for specific inductors or capacitors, corresponding capacitance or inductance should be set to fixed parameters, and V&A ratings should also be updated accordingly. The optimization process then has to be repeated for all combinations of components, and multiple loss-volume tradeoff curves will be generated to determine the final Pareto front. For example, two other inductors listed in Table. VIII have been selected to compare with the optimization result in Fig. 10 obtained with the Vishay IHLP6767 inductor. The volume of the inductors are added to the total volume function. The result of such optimization are shown in Fig. 23.

TABLE VII
DESIGN PARAMETERS OF PREVIOUS HARDWARE DEMONSTRATION

	Hardware in [3, 4]	Hardware in [11, 13]	Hardware in [19]
Rated dc-side power	2 kW	500 W	750 W
Dc-bus voltage	400 V	200 V	200 V
Line Frequency	60 Hz	50 Hz	60 Hz
C_1 volume (types)	19.1 cm^3 (MLCC X6S)	86.3 cm^3 (Film)	86.3 cm^3 (film)
Equivalent large-signal capacitance for C_1 @ 400 V	100 μF	100 μF	100 μF
C_2 volume (types)	9 cm^3 (MLCC X7S)	9 cm^3 (E-cap)	10.85 cm^3 (E-cap)
Equivalent large-signal capacitance for C_2 @ $V_{C2,\,dc}$	430 μF	470 μF	440 μF
$V_{C2,\,dc}$ at full load	81 V	60 V	60 V
L_f volume (specs)	4.1 cm^3 (94 μH, 8.6 A)	34.3 cm^3 (100 μH, 3 A)	3.3 cm^3 (44 μH, 6.1 A)
Power density by component volume (C_1,C_2,L_f)	62.1 W/cm^3	3.85 W/cm^3	7.47 W/cm^3
2-port efficiency @ full load	99.3%	Not Reported	Not Reported

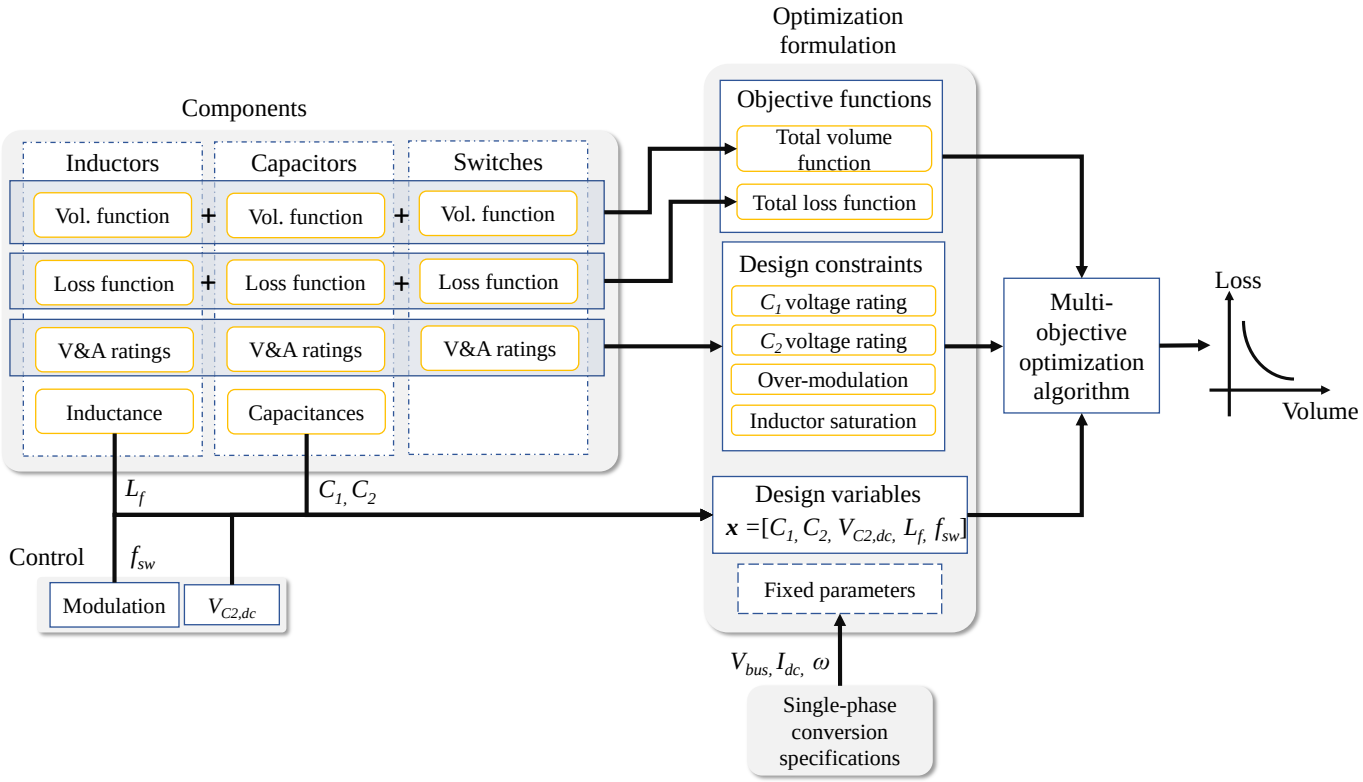

Fig. 22. Design flow chart with generalized optimization methodology.

TABLE VIII
INDUCTORS FOR COMPARISON

Part No.	Inductance	I_{sat}	DCR	Volume
IHLP6767	47 μH	8.6 A	0.04 Ω	2.06 cm^3
IHLP4040	47 μH	4.5 A	0.17 Ω	0.47 cm^3
IHLP5050	15 μH	14.5 A	0.03 Ω	1.14 cm^3

The algorithm to solve the multi-objective optimization (MOO) problem is not limited to Weighted Sums method. Different methods to solve continuous nonlinear MOO problem can be applied, depending on the types of information provided for setting up the problem [20].

To further expand the scopes of the optimization, reliability and cost objective functions [11] can also be adopted in the optimization procedure for cost-effective and reliability-oriented analysis. The volume of the heatsink can be modeled from the loss and switch volume and added to the total volume function to optimize the overall electro-thermal system solution [27].

Behavior during load transient events can also be incorporated. In general, more energy stored in the capacitors will provide higher margin to handle transient events [8]. While the exact voltage and current waveforms also depend on the rest of the system, the total stored energy in C_1 and C_2 can be studied as an objective function to indicate the buffer's ability to handle transient events.

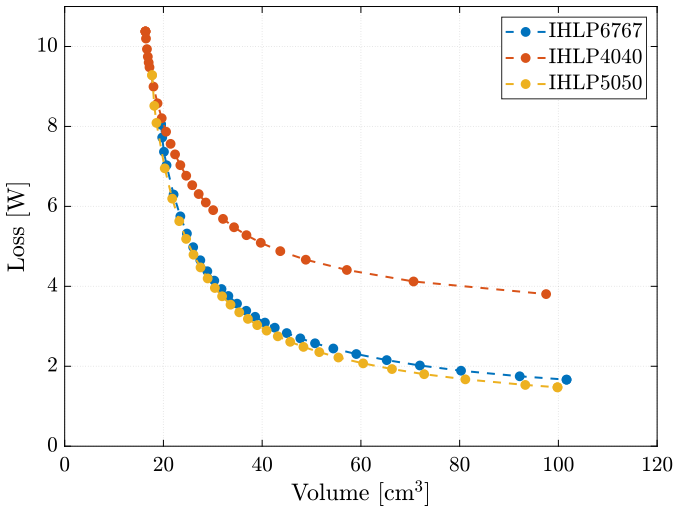

Fig. 23. Calculated Pareto Front with three different inductors.

VIII. Conclusion

A methodology to optimize the loss and volume of the SSB is proposed. With updated operating constraint, the energy utilization of the energy buffering capacitors are optimized. The performance of the SSB hardware prototypes designed based on the Pareto front matches the calculated optimal results, which further verifies the effectiveness of the proposed models and optimization process. The Pareto front and the optimized hardware prototypes have identified large space for improvement in both power density and efficiency compared to previous SSB hardware prototypes. Furthermore, the proposed methodology provides a framework to link component properties to the operating constraints and the objective functions, which can be generalized to involve more design variables and objectives for the optimization.

IX. Appendix

A. Relation between bus voltage ripple and loss compensation

From the control diagram in Fig. 13, the loss compensation voltage term is orthogonal to the primary control path and in-phase with the buffer current. Thus, the loss compensation voltage term can be expressed as

$$v_{\text{ab, com}} = -V_{\text{com}} \sin(\omega t). \tag{34}$$

As the primary control path is canceling the ripple on C_1, the final reference voltage $v_{\text{ab, ref}}$ is

$$v_{\text{ab, ref}} = -\Delta v_{\text{C1}} + v_{\text{ab, com}} \tag{35}$$

Assuming the actual v_{ab} equals the reference voltage $v_{\text{ab, ref}}$, the dc-bus voltage equals to

$$\begin{aligned} v_{\text{bus}} = v_{\text{C1}} + v_{\text{ab}} &= (V_{\text{bus}} + \Delta v_{\text{C1}}) + (-\Delta v_{\text{C1}} + v_{\text{ab, com}}) \\ &= V_{\text{bus}} + v_{\text{ab, com}} \end{aligned} \tag{36}$$

Thus, the ripple component on the dc-bus is exactly $v_{\text{ab, com}}$. The dc-side source current then becomes

$$i_{\text{s}} = \frac{V_{\text{S}} - v_{\text{bus}}}{R_{\text{S}}} = \frac{V_{\text{S}} - V_{\text{bus}} - v_{\text{ab, com}}}{R_{\text{S}}} = I_{\text{dc}} - \frac{v_{\text{ab, com}}}{R_{\text{S}}} \tag{37}$$

Following the current constraint at the dc-bus voltage in (2), the updated buffer current including the loss compensation current is then

$$i_{\text{buf, com}} = -I_{\text{dc}} \sin(\omega t) + \frac{v_{\text{ab, com}}}{R_{\text{S}}} \tag{38}$$

The average real power for loss compensation into the full-bridge converter within one 120 Hz cycle can be calculated based on the analysis in [4] as

$$P_{\text{loss}} = \frac{\omega}{2\pi} \int_0^{1/120} v_{\text{ab}} i_{\text{buf, com}} \, dt \tag{39}$$

which can be further simplified to

$$P_{\text{loss}} = \frac{V_{\text{com}}}{2} (I_{\text{dc}} + \frac{V_{\text{com}}}{R_{\text{S}}}) \tag{40}$$

Equation (40) can be rearranged as a quadratic equation with variable V_{com}, whose solution can be found as

$$V_{\text{com}} = \frac{-I_{\text{dc}} R_{\text{S}} + \sqrt{(I_{\text{dc}} R_{\text{S}})^2 + 8 P_{\text{loss}} R_{\text{S}}}}{2} \tag{41}$$

Since the peak-to-peak bus voltage ripple $\Delta v_{\text{bus, pk-pk}} = 2V_{\text{com}}$, Eq. (30) is obtained.

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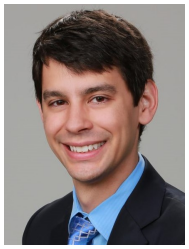

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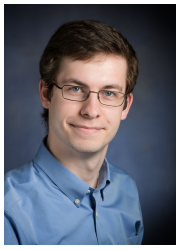

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