Design and Implementation of a High Power Density Bipolar Multi-Level Active Power Pulsation Buffer for Single-Phase Converters

Abstract

Active power decoupling methods in single-phase systems aim to reduce the required capacitance for twice-line frequency power ripple buffering, with extra power converters to improve the energy utilization ratio of the capacitors. While many active buffer solutions can improve the energy utilization ratio of the capacitor to a certain extend and reduce the required capacitance, they require the use of high energy density ceramic capacitors to achieve comparable power density against the passive electrolytic capacitor bank solution. The ceramic capacitors have to be carefully assembled and packaged, and they are also costly and heavy in weight. In this work, a bipolar ripple port converter, which allows the use of the minimum buffering capacitance in single-phase conversion with 100% energy utilization ratio, is implemented with metal film capacitors, and two flying capacitor multilevel (FCML) legs operated as a full-bridge to shrink the filter inductor size and improve efficiency. A compact hardware and digital control scheme are implemented. Experimental results demonstrating the active power ripple decoupling at 2 kW, 400 V dc bus are provided and discussed.

I. Introduction

In single-phase ac-dc or dc-ac system, large dc-link capacitors are usually required to buffer the twice-line frequency pulsating power mismatch between the dc side and the ac side. However, due to the small dc-bus ripple requirement, the energy utilization ratio of the capacitor is very low, leading to large physical size. Active decoupling methods in general improve the energy utilization ratio of the capacitors by allowing larger voltage ripple on the capacitors, while decoupling such large ripple from the dc bus voltage with the help of extra power converters.

The bipolar ripple port converter in [1] is a type of active decoupling solution that applies a line frequency sinusoidal voltage onto a buffer capacitor with a full-bridge converter to provide the reactive power for active decoupling. Because the buffer capacitor is fully discharged to zero volt at every zero crossing of the sinusoidal voltage, the energy utilization ratio is 100%. If the buffer capacitor voltage swings with the amplitude up to the full bus voltage, the required capacitance for decoupling is minimized. However, because of the high voltage stress and high RMS current through the buffer capacitor, implementing the full-bridge converter with a conventional two-level design suffers from large filter inductor size, high voltage stress on the switches, and higher device count compared to half bridge unipolar ripple port. As a result, high loss and large inductor size usually offset the benefit of the small capacitance for the conventional two-level bipolar ripple port.

To shrink the converter size and improve efficiency, different active decoupling solutions have been proposed improving upon the bipolar ripple port converter. However, they generally incur a trade-off of lower energy utilization ratio of the capacitor. For example, the unipolar half-bridge power pulsating buffer [2] has half the device count of the full-bridge bipolar ripple port. To avoid high current slew rate and high peak current in the actual implementation, the buffer capacitor has to hold high dc bias such that the inductor current is continuous and has lower amplitude, which lowers the energy utilization ratio and requires higher buffer capacitance as a trade-off. Other solutions such as the series-stacked buffer (SSB) configuration [3], [4] reduces the power processed by the full-bridge converter to reduce the overall loss by connecting a bulk capacitor in series to block the high dc-bus voltage. However, the main buffering bulk capacitor is biased with the dc-bus voltage, which means the allowed ripple is limited by the voltage rating of the physical capacitor. As a result, higher total buffer capacitance is also needed. In

the practical design of [2] and [3], [4], the energy utilization ratio of buffer capacitors are below 50%. To achieve high power density with higher buffer capacitance, instead of using low-energy-density film capacitors, many single high-energy-density multi-layer ceramic capacitors (MLCC) are connected in parallel and packaged as large capacitor blocks. While MLCCs brings benefits such as high power density and efficiency, they are also very sensitive to mechanical and thermal shocks, as they would cause cracks inside the ceramic layers and lead to various electrical defects or failures [5]. Such properties of MLCC require advanced packaging process to ensure performance and limit the operating conditions and environment of the converter.

In this work, we seek to overcome the limitations of the conventional bipolar ripple port converter, by implementing it with two Flying Capacitor Multilevel (FCML) converters. With FCML, the filter inductor size and the overall passive component volume in the converters are much reduced. The high efficiency and high power density characteristics of the FCML has been demonstrated in [6]. Furthermore, because of the high energy utilization ratio of the capacitor, high overall power density can be achieved with metal film capacitors as the buffer capacitor. A full control scheme with voltage regulation and harmonic compensation is implemented with a digital controller to minimize the dc-side current ripple and enables passive component size reductions and minimum loss. The proposed buffer topology, control and modulation schemes are implemented and verified with a compact hardware prototype, and experimental test results up to 2 kW for 400 V dc bus are provided in this digest.

II. Principle of Operation of the Proposed Buffer topology

The schematic drawing of the proposed bipolar multi-level active power pulsation buffer within an exemplar dc-ac system is shown in Fig. 1. The dc source is modeled as a voltage source V_s with a source resistance R_s. For simplicity, ac side with unity power factor is considered in this digest. With unity power factor, the inverter load can be represented as a dc-shifted twice-line frequency current load at the dc-bus i_{inv} in (1). In ideal operation for active decoupling, the current flowing into the buffer branch i_{buf} has to cancel the sinusoidal part of i_{inv}, i.e., $i_{\text{buf}} = I_{\text{dc}} sin(2\omega_L t)$.

The differential equation that describes the power balance of the buffer converter in (3) has to be solved to find the expression for v_{CB}. With zero dc bias on C_{buf}, v_{CB} is found as in (4), where V_{CB} is the magnitude. The ideal waveforms of i_{inv}, i_{buf}, i_{dc} and v_{CB} are plotted in Fig. 2. From (4), we can also derive the minimum capacitance needed for given single-phase conversion conditions as in (5), where P_0 is the single-phase system power, V_{bus} is the dc-bus voltage and ω_L is the line angular frequency.

To generate the correct v_{CB}, two 6-level FCML legs are implemented as a full-bridge, where the output v_{CB} equals the differential output of two FCML legs as in (2). The conversion ratio of the FCML is identical to a conventional two-level buck. Operated with phase-shifted PWM (PSPWM), the inductor size of the FCML is reduced by $(N-1)^2$ times compared to a two-level buck converter (N is the number of levels) to the first-order estimation[6], [7], [8].

$$i_{\text{inv}} = I_{\text{dc}} - I_{\text{dc}} sin(2\omega_L t) \quad (1)$$

$$v_{\text{CB}} = m V_{\text{bus}} = (D_1 - D_2) V_{\text{bus}} \quad (2)$$

$$V_{\text{bus}} i_{\text{buf}} = C_{\text{buf}} v_{\text{CB}} \frac{\mathrm{d}v_{\text{CB}}}{\mathrm{d}t} \quad (3)$$

$$v_{\text{CB}} = V_{\text{CB}} sin(\omega_L t) = \sqrt{\frac{2V_{\text{bus}} I_{\text{dc}}}{\omega_L C_{\text{buf}}}} sin(\omega_L t) \quad (4)$$

$$C_{\text{buf, min}} = \frac{2P_0}{\omega_L V_{\text{bus}}^2} \quad (5)$$

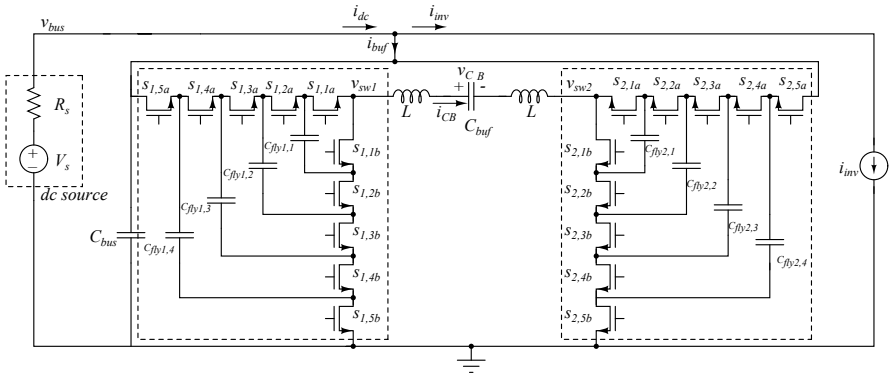

Fig. 1. Schematic drawing of the proposed buffer topology with key components, voltage and current annotated.

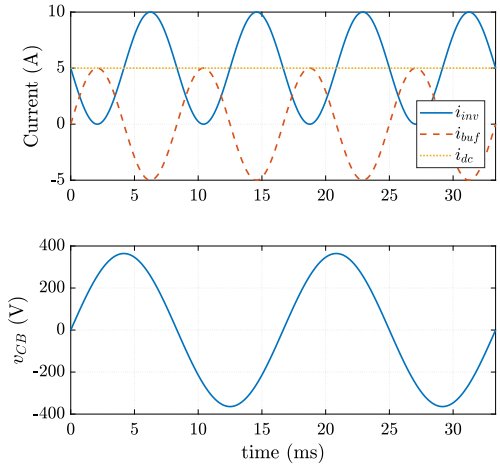

Fig. 2. Ideal waveforms of the proposed buffer operation with 400 V dc-bus, 2 kW system power, and 80 μF buffer capacitance.

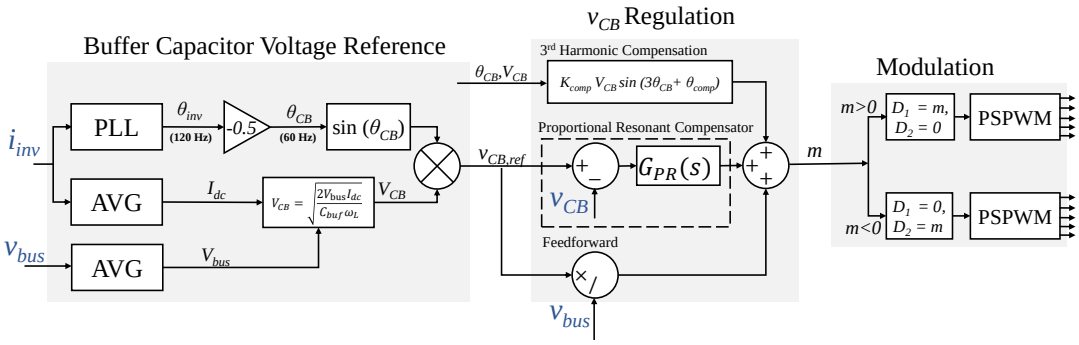

Fig. 3. Block diagram of the proposed active decoupling control and modulation strategies. The sensed parameters are in the blue font.

III. Control of Buffer Capacitor Voltage

The full control scheme of the buffer converter is shown in Fig. 3. It consists of mainly three parts: generating ideal voltage reference for buffer capacitor voltage v_{CB}, regulation and modulation.

A. Buffer capacitor voltage v_{CB} reference

From (1) and (4), the angle relation between the inverter current and buffer voltage can be determined. If the angle of the inverter current is $\theta_{\mathrm{inv}} = -2\omega_L t$, the angle for the buffer capacitor voltage is then $\theta_{\mathrm{CB}} = \omega_L t = -0.5\theta_{\mathrm{inv}}$. To generate low-harmonic and low-noise reference voltage for the buffer capacitor, a Phase-Locked Loop (PLL) based control is implemented as shown in Fig. 3. The inverter current i_{inv} is sensed, and a PLL based on digital notch filters is designed to detect the angle θ_{inv}. Once θ_{CB} is calculated from θ_{inv}, the magnitude V_{CB} can be calculated based on (4). To do so, the average dc current I_{dc} is obtained by averaging i_{inv}, and the dc-bus voltage V_{bus} is also sensed and calculated. Assuming C_{buf} is implemented with linear capacitors, C_{buf} and ω_L are known parameters to the system. The square-root function in the DSP controller (TI C2000 Delfino) can then be used to calculate V_{CB}.

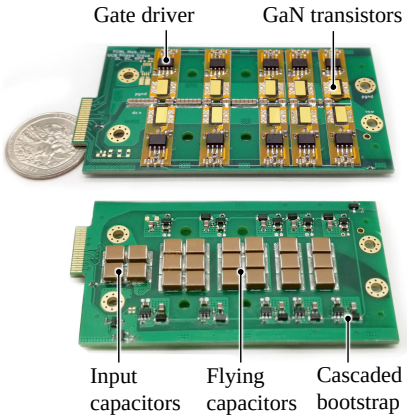

Fig. 4. Photos of the top and bottom view of the FCML module used in the buffer converter with key components annotated, and a U.S. quarter for size reference.

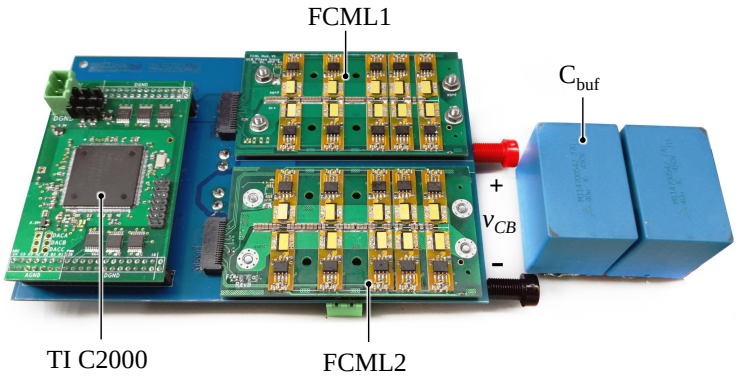

Fig. 5. The hardware prototype assembly with key components annotated.

B. Regulation of v_{CB}

The voltage swing on v_{CB} becomes larger as load increases. Any distortion of the actual v_{CB} will result in discrepancy between the actual buffer current and the ideal buffer current $I_{\text{dc}} sin(2\omega_L t)$, which means the ripple component in i_{inv} will not be perfectly canceled. As a result, there will be unwanted ripple component in the dc-side current, which is usually restricted to a certain limit ($\leq$ 20%) for many practical applications [9]. To obtain a low-harmonic v_{CB}, a regulation scheme with feedforward, a Proportional-Resonant (PR) compensator [10], and third-harmonic compensation is implemented [11]. Details on the design of compensators will be provided in the full paper. The effectiveness of the proposed regulation scheme will be shown with experiment waveforms in later sections.

C. Modulation of two FCML legs

Once v_{CB} is determined from the active power decoupling control, the two FCML legs have to be modulated with D_1 and D_2 to generate the correct differential conversion ratio m. It has been shown in [12] that to generate the sinusoidal voltage of v_{CB}, the leg-alternating modulation scheme will result in the least amount of circulating power, leading to lowest loss. As the modulation scheme shown in Fig. 3, one FCML leg is shorted to ground while the other leg modulates with PSPWM, alternating each half cycle.

IV. Hardware and Experimental Results

The FCML portion of the buffer is implemented with the 6-level FCML module in Fig. 4. The full buffer hardware prototype is constructed with two FCML modules mounting on a control and sensing board as shown in Fig. 5. The FCMLs are designed with 100 V GaN System FETs, isolated gate drivers and cascaded bootstrap method for float gate driving power [13]. The buffer capacitors used in the experiment are two 450 V, 40 μF metal film capacitor TDK B32776G4406K, and the filter inductors are two 6.8 μH Vishay IHLW5050 inductors. Accounting for the volume of all the passive components (C_{bus}, C_{buf}, filter inductors, flying capacitors) in the main

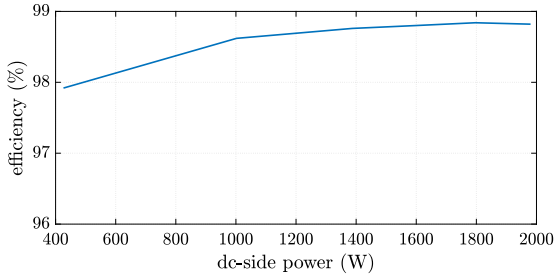

Fig. 8. Efficiency plot with 400 V dc bus, up to 2 kW system power. Peak efficiency is 98.84% at 1.8 kW, and 98.82% at 2 kW.

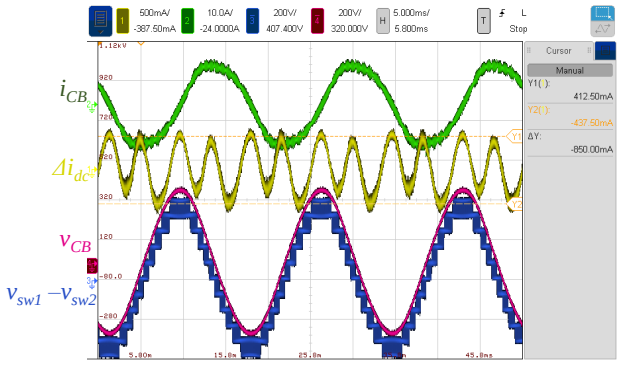

Fig. 6. Experimental waveforms of the proposed buffer controlled with only feedforward and PR compensator. The dc source current i_{dc} is ac-coupled to showcase the ripple component. Test condition: 400 V dc bus, 2 kW dc power.

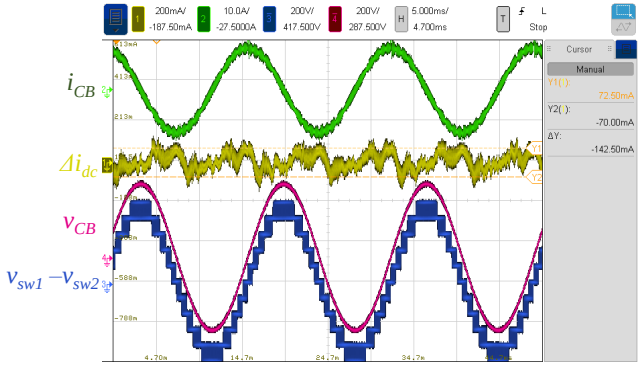

Fig. 7. Experimental waveforms of the proposed buffer controlled with additional 3rd harmonic compensation, along with feedforward and PR compensator. The dc source current i_{dc} is ac-coupled to showcase the ripple component. As shown, the dc-side current has much lower ripple component with 3rd harmonic compensation. Test condition: 400 V dc bus, 2 kW dc power.

power stage, the power density of the hardware by passive component volume is 21.6 W/cm^3 (354 W/in^3). The volume breakdown of each passive components are listed in Table. I. It should be noted that this prototype employed long-lifetime metal film capacitors, which are required in many automotive applications. If ceramic capacitors would have been used, the overall power density would be approximately three times higher. Detailed component list will be given in the full paper.

The experimental setup includes a dc voltage source of 450 V, a 10 Ω source resistor, and an electronic load operated in current load mode to emulate an inverter load with unity power factor. The buffer converter is tested up to 2 kW with no heatsink, and the efficiency is measured with Keysight PA2201A power analyzer, which is plotted in Fig. 8. The peak efficiency is 98.84% at 1.8 kW, and 98.82% at 2 kW. Figure 6 and Fig. 7 show the steady-state operation under the condition of 400 V dc-bus, and 2 kW dc power. Dc source current i_{dc}, buffer capacitor voltage v_{CB} and i_{CB} and the differential FCML switching node voltage $v_{\text{sw1}} - v_{\text{sw2}}$ are monitored. As can be seen in Fig. 6, with only feedforward and PR compensator, the buffer capacitor's voltage and current are obviously distorted, and the buffer converter is not able to perfectly cancel the twice-line frequency component in i_{inv}, resulting in 850 mA ripple on the dc-side current. With additional 3rd harmonic compensation term, the buffer capacitor voltage is less distorted, and the resulting ripple component in the dc-side current is reduced to 142.5 mA, as shown in Fig. 7. The corresponding ripple current ratio is 2.9%, which is significantly lower than the common limit of 20%. This ripple ratio is equivalent to having 9.3 mF physical capacitor at the dc-bus, if passive capacitor bank solution is used. More experimental results on different load transients and under higher power will be provided in the full paper.

TABLE I

VOLUMES OF PASSIVE COMPONENTS

Passive Components	Volume (cm^3)
C_{buf}	87.02
C_{fly}	2.87
C_{bus}	1.60
L	1.13

V. CONCLUSION

The proposed bipolar multi-level active power pulsation buffer allows the use of the minimum buffer capacitance, while shrinking the switching-frequency filtering passive component size with FCML topology. The proposed active decoupling control scheme is able to determine the correct buffer capacitor voltage, achieving 2.9% ripple ratio on the dc source current, 98.84% peak efficiency under the tested load condition, and 21.6 W/cm^3 power density by component volume.

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